ARINC 825

Standard CAN Bus Protocol for Airborne Use

Support for esdACC based CAN FD Boards

Wide Range of Scheduling

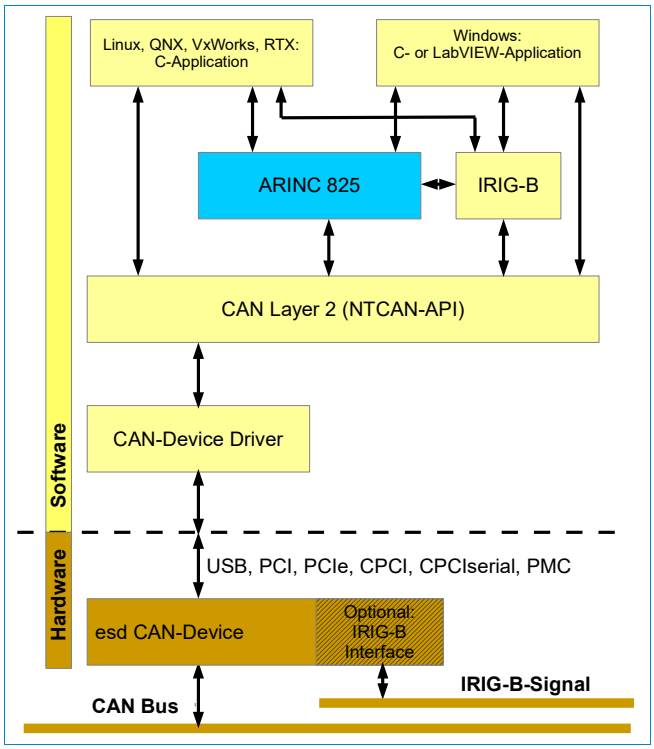
- *Minor Time Frame scheduling with timer resolution < 1 µs*
- *Number of Minor Time Frames not limited*
- *Minor Time Frame period ≥ 2 ms*
- *Scheduling starts at dedicated time*

Implementation for different Applications

- *Implementation according to ARINC Specification 825-4 (This version, supplement 4, includes CAN FD support)*
- *Available for many operating systems such as Windows®, Linux®, QNX®, RTX, RTX64 and VxWorks®*
- *C- and LabVIEW API available*
- *Support of different hardware platforms*

Realtime Behaviour for Non-Realtime Systems

- *Time base for hardware scheduling*
- *Timer synchronization based on IRIG-B signal available*
- *Tx-abort at the Minor Time Frame end with response*



Timing

The timing source of the ARINC 825 library is the hardware timer of an esdACC based CAN device. This makes the timing highly precise. Scheduling of the Minor Time Frames is extremely precise and accurate. For non-realtime systems like Linux or Windows, the hardware timer gives an decisive advantage, especially for CAN-USB devices, which otherwise cannot be ideally integrated due to the cyclic USB protocol.

A timer resolution of less than 1 µs and a Minor Time Frame period down to 2 ms, opens a large application field for the ARINC 825 library.

Synchronization

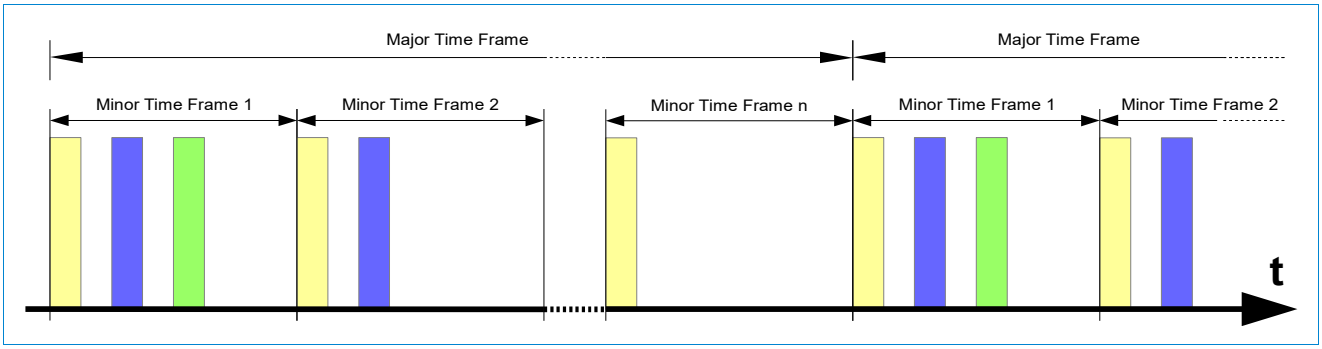
esd offers esdACC CAN and CAN FD devices with IRIG-B input for many hardware platforms. This offers time synchronization for an unlimited number of systems and between different hardware platforms.

Hardware Requirements

Hardware platform of the ARINC825 protocol library are all esd CAN devices which are equipped with the esd CAN-IP-Core esdACC, USB, PCI, PCIe, PCIeMini, CompactPCI®, CompactPCI Serial, PMC and XMC interfaces are available.

Programming Interface

A C-API is available for the operating systems Windows, Linux, VxWorks, QNX, RTX and RTX64. On Windows operating systems, LabVIEW applications can also use the ARINC 825 library.



Technical Specifications:

Requirements:		
Hardware	*esdACC based esd CAN device, for example:*	
	PCI Express:	*CAN-PCIe/402(-FD)*
	PCI Express Mini:	*CAN-PCIeMini/402-2-FD,*
	PCI:	*CAN-PCI/402(-FD)*
	PMC:	*PMC-CAN/402-4-FD(-IRIG-B)*
	XMC:	*XMC-CAN/402-4-FD(-IRIG-B)*
	CompactPCI:	*CPCI-CAN/402-4(-FD)*
	CompcatPCI Serial:	*CPCIserial-CAN/402-4-FD (-IRIG-B)*
	USB:	*CAN-USB/400(-FD)*
Operating Systems	*Windows, Linux, VxWorks, QNX, RTX, RTX64*	
Programming interface	*- C-API* *- LabVIEW (Windows operating system only)*	

Order Information:

Description		*Order No.*
	CD ROM + Licence for ...	
ARINC825 WIN	*Windows, Linux, LabVIEW*	*C.1140.06*
ARINC825 QNX	*QNX*	*C.1140.17*
ARINC825 RTX	*RTX, RTX64*	*C.1140.16*
ARINC825 VxW	*VxWorks*	*C.1140.18*

CAN layer 2 drivers for Windows and Linux are included in delivery.
For detailed information about driver availability for your operating system please contact our sales team.

esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu

ARINC 825

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1:2015 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Test
  "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Supported bit rates:
  CAN interfaces: From 10 kbit/s up to 1 Mbit/s
  CAN FD interfaces: From 10 kbit/s up to 5 Mbit/s
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Self-reception mode (reception of 'own' messages)
- Busload measurement

Superior esdACC Features [1]:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  - Timestamping complies with the CiA 603 specification
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64-bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - E.g. for driver timeouts
  - ISO11898-1:2015 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
  - The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.

esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu