CPCIserial-CAN/402-4-FD

CompactPCI® Serial Board with 4x CAN FD, optional IRIG-B Input

CompactPCI Serial Board with FPGA for 4x CAN FD via DSUB25

- High-Speed CAN FD interfaces acc. to ISO 11898-2, up to 8 Mbit/s
- Bus mastering and local data management by FPGA (esdACC)
- PICMG® CPCI-S.0 standard supporting high speed PCI Express® interface lines
- Selectable CAN termination on board
- Supports MSI (Message Signaled Interrupts)
- All I/O signals via 25-pin DSUB in the front panel
- Optional IRIG-B inputs

- **Wide Range of OS Support and Advanced CAN Diagnostic**
- Software drivers for Windows® and Linux® included free of charge
- Optional CAN layer 2 software drivers for real-time operating systems
- CANopen®, J1939 and ARINC 825 protocol libraries
- ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology
- High resolution hardware timestamps

Advanced CAN Controller

- esdACC technology offers highest CAN performance and diagnostic

Customization on Request

- Ext. temperature range: -40° C … +75° C
- Error simulation support
- All signals via Rear I/O (P3)

CAN FD

The CPCIserial-CAN/402-4-FD comes with four independent CAN FD interfaces via DSUB25 according to ISO 11898-1.
The CAN FD interfaces are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core) implemented in the FPGA.
With a higher bit rate in the data phase in combination with the increase of efficiency by a higher number of user-data bytes, CAN FD offers a higher data throughput while maintaining the benefits of Classical CAN.
CPCIserial-CAN/402-4-FD is fully backwards compatible with CAN and can also be used in Classical CAN applications.

CAN Data Management

The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load.
Due to the usage of MSI (Message Signaled Interrupts) the CPCIserial-CAN/402-4-FD can be operated for example in Hypervisor environments.
The CPCIserial-CAN/402-4-FD provides high resolution 64-bit hardware timestamps for CAN messages

IRIG-B

An additional IRIG-B interface is equipped on the CPCIserial-CAN/402-4-FD-IRIG-B. It offers inputs for analog or RS-422 IRIG-B coded signals. Both are electrically isolated. IRIG-B evaluation is controlled by an 8051 microcontroller integrated in the FPGA.

Software Support

Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Realtime OS (NTCAN-API)
CAN layer 2 drivers e.g. for QNX®, RTX64®, VxWorks® can be ordered separately.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for many operating systems (see order info):

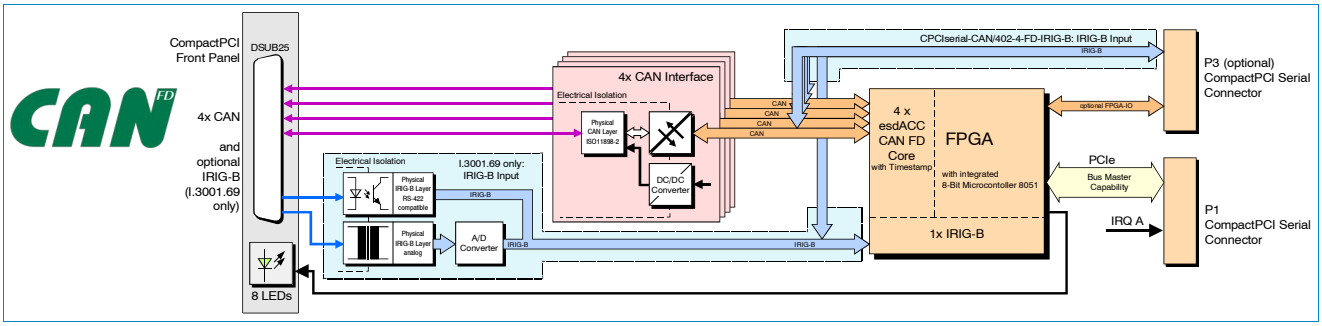
- CANopen Master- and Slave-Stack
- J1939
- ARINC825

Customization on Request

Customized options are available for customized serial production in reasonable quantities. Please contact our sales team for detailed information.

Related Products

The CPCIserial-CAN/402-2-FD board provides 2 CAN FD interfaces via DSUB9.



Technical Specifications:

CompactPCI Serial:	
PCI	PICMG CPCI-S.0 Rev. 1.0, PCI Express Rev. 1.0a, Link width 1x
Interfaces:	
CAN interface	4x interface according to ISO11898-2, bit rates from 10 Kbit/s up to 8 Mbit/s, CAN termination selectable via jumper, electrical isolation (1000 V, 1 s)
CAN controller	esdACC in EP4CGX Intel FPGA, ISO 11898-1
IRIG-B input	Physical layer for analog or RS-422 IRIG-B coded signals
General:	
Ambient temp.	Operation: 0 °C ...+75 °C / Storage: -40 °C ...+85 °C
Rel. humidity	Max. 90 % (non-condensing)
Power supply	12 V; 4x CAN: I_{MAX_12V} = 250 m A, P_{MAX_12V} = 3 W
Connector	CompactPCI Serial P1: CompactPCI Serial interface, acc. to PICMG CPCI-S0 Rev. 1.0 DSUB25 connector: 4x CAN FD, pin contacts IRIG-B (I.3001.69 only)
Weight	150g
Mechanics	3 U / 4 HP, compliant to IEEE 1101
LEDs	8 LEDs, CAN status, module status

Order Information:		
Hardware		*Order No.*
CPCIserial-CAN/402-4-FD	4x CAN FD via 1x DSUB25, 4 HP	I.3001.68
CPCIserial-CAN/402-4-FD-IRIG-B	as I.3001.68, + IRIG-B input	I.3001.69
Accessories		
CAN/400-4-1C4	For I.3001.68: Cable DSUB25 to 4x DSUB9 plug	C.2047.19
CAN/400-4-1C5	For I.3001.69: Cable DSUB25 to 4x DSUB9 pin contacts,1x DSUB9 socket contacts	C.2047.18
Software Support[1]		
CAN layer 2 drivers for Windows/Linux are included in delivery free of charge.		
Additional CAN layer 2 object licences including CD-ROM:		
CAN-DRV-LCD QNX	Object licence for QNX6, QNX7	C.1101.32
CAN-DRV-LCD RTX	Object licence for RTX64	C.1101.35
CAN-DRV-LCD VxWorks	Object licence for VxWorks	C.1101.55
Higher CAN layer protocols including CD-ROM for Classical CAN Application:		
CANopen-LCD Windows/Linux, QNX, RTX or VxWorks		C.1101.xx
J1939 stack for Windows or Linux		C.1130.xx
ARINC 825-LCD for Windows/Linux, QNX, RTX or VxWorks		C.1140.xx
Related Products:		
CPCIserial-CAN/402-2-FD	2x CAN FD via 2x DSUB9, 4 HP	I.3001.64

[1] *For detailed information about driver availability for your operating system please contact our sales team.*

esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu

CPCIserial-CAN/402-4-FD

Driven by esdACC-FD (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Supported bit rates from 10 kbit/s up to 8 Mbit/s
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Disable Automatic Retransmission (DAR) (Single-shot transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Self-reception mode (reception of 'own' messages)
- Busload measurement

Superior esdACC Features [1]:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  - Timestamping complies with the CiA 603 specification
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO 11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.

esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu