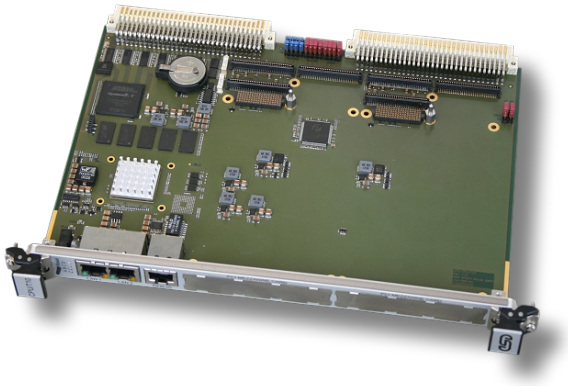
VME-CPU/T10

VME Master with 64-bit PowerPC™ T1022, XMC/PMC Slots

VME-CPU/T10-F

VME Master with 64-bit PowerPC™ T1014



VME-CPU/T10

Hardware Manual

to Product V.1940.01,
V.1940.02

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N O T E

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This manual contains important information and instructions on safe and efficient handling of the VME-CPU/T10. Carefully read this manual before commencing any work and follow the instructions.
The manual is a product component, please retain it for future use.

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Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Rev.	Chapter	Changes versus previous version	Date
1.0	-	First English manual	2016-12-02
1.1	1.2	Text about customized digital IO expansion of health controller deleted	2017-01-18
	7.6.5	Correction of description: Pin-out conforms with P4V2-46dz	
	13	Order information for BSP-Support supplemented	
1.2	1.2	Block circuit diagram without optional MCU (Health)	2018-11-14
	2.1.1	PCB top layer view (with PMV voltage keying pins)	
	2.3.4	Note on voltage keying pins inserted	
	3.2.1	Note on default settings inserted	
	3.2.2	Note on default settings inserted	
	3.2.3	New chapter ”PMC voltage Keying Pins”	
	4.	Description of installation step 5 revised.	
	7.8	Description of XMC-CPU-ADAPTER-NXP deleted	
	13.	Order Information of VME-CPU/T10-Cable_Console inserted, CPU-ADAPTER-NXP removed	
1.3		Note on declaration of conformity added under safety instructions	2019-03-01
	2.3.4	Note on Mezzanine filler panels inserted	
	4.	Note on Mezzanine filler panels and conductive O-ring added	
	7.1	Note on cable added	
	9.2	Cross-references corrected	
	13.	New chapter: “EU-Declaration of Conformity”	
1.4	1.3	Block circuit diagram corrected: CPU QorIQ T1014	2021-08-24
	5.2	Table supplemented, CPU: NXP QorIQ T1022 (VME-CPU/T10) or T1014 (VME-CPU/T10-F)	

Technical details are subject to change without further notice.

Classification of Warning Messages and Safety Instructions

This manual contains noticeable descriptions, warning messages and safety instructions, which you must follow to avoid personal injuries or death and property damage.

This is the safety alert symbol.
It is used to alert you to potential personal injury hazards. Obey all safety messages and instructions that follow this symbol to avoid possible injury or death.

DANGER, WARNING, CAUTION

Depending on the hazard level the signal words DANGER, WARNING or CAUTION are used to highlight safety instructions and warning messages. These messages may also include a warning relating to property damage.

DANGER
Danger statements indicate a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING
Warning statements indicate a hazardous situation that, if not avoided, could result in death or serious injury.

CAUTION
Caution statements indicate a hazardous situation that, if not avoided, could result in minor or moderate injury.

NOTICE

Notice statements are used to notify people on hazards that could result in things other than personal injury, like property damage.

NOTICE
This NOTICE statement indicates that the device contains components sensitive to electrostatic discharge.

NOTICE
This NOTICE statement contains the general mandatory sign and gives information that must be heeded and complied with for a safe use.

INFORMATION

INFORMATION
Notes to point out something important or useful.

Safety Instructions

- When working with the VME-CPU/T10 follow the instructions below and read the manual carefully to protect yourself from injury and the VME-CPU/T10 from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- Do not use damaged or defective cables to connect the VME-CPU/T10.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The VME-CPU/T10 may only be driven by power supply current circuits, that are contact protected. A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with this conditions.

- The device has to be securely installed in the control cabinet before commissioning.
- Protect the VME-CPU/T10 from dust, moisture and steam.
- Protect the VME-CPU/T10 from shocks and vibrations.
- The VME-CPU/T10 may become warm during normal use. Always allow adequate ventilation around the VME-CPU/T10 and use care when handling.
- Do not operate the VME-CPU/T10 adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.

DANGER
Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the VME-CPU/T10 is to be integrated.

→ All current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1) before you start with the installation.
→ Ensure the absence of voltage before starting any electrical work

DANGER
Risk of personal injury due to explosion or leakage of the battery!
Improper usage of the battery such as overheating, short-circuiting or mechanical damage may cause an explosion or leakage.

→ Do not replace the battery by an incorrect type.
→ Do not recharge the battery.
→ Insert the battery properly, with the +/- terminals correctly oriented.
→ Dispose used batteries according to the national instructions.

NOTICE
Electrostatic discharges may cause damage to electronic components.
To avoid this discharge the static electricity from your body *before* you touch the VME-CPU/T10.

Qualified Personnel

This documentation is directed exclusively towards personnel qualified in control and automation engineering. The installation and commissioning of the product may only be carried out by qualified personnel, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity

The VME-CPU/T10 is an industrial product and meets the demands of the EU regulations and EMC standards printed in the conformity declaration at the end of this manual.
Warning: In a residential, commercial or light industrial environment the VME-CPU/T10 may cause radio interferences in which case the user may be required to take adequate measures.

The VME-CPU/T10 is a sub-assembly intended for incorporation into an apparatus. The manufacturer of the final system must decide, whether additional EMC or EMI protection requirements are necessary.

Data Safety

This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.
esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

Intended Use

The intended use of the VME-CPU/T10 is the operation as VME Master with 64-bit PowerPC™ T1022, XMC/PMC Slots.
The VME-CPU/T10-F is a customized version of the VME-CPU-board with NXP® QorIQ® T1014 processor.
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The VME-CPU/T10 is intended for installation in a VME system only.
- The operation of the VME-CPU/T10 in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the VME-CPU/T10 for medical purposes is prohibited.

Service Note

The VME-CPU/T10 does not contain any parts that require maintenance by the user. The VME-CPU/T10 does not require any manual configuration of the hardware. Unauthorized intervention in the device voids warranty claims.

Disposal

Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

Typographical Conventions

Throughout this manual the following typographical conventions are used to distinguish technical terms.

Convention	Example
File and path names	**`/dev/null`** or **`<stdio.h>`**
Function names	***open()***
Programming constants	`NULL`
Programming data types	`uint32_t`
Variable names	*Count*

Number Representation

All numbers in this document are base 10 unless designated otherwise. Hexadecimal numbers have a prefix of 0x. For example, 42 is represented as 0x2A in hexadecimal.

Abbreviations

API	Application Programming Interface
CPU	Central Processing Unit
HW	Hardware
I²C	Inter-Integrated Circuit
I/O	Input/Output
n.a.	not applicable
OS	Operating System
PCIe	Peripheral Component Interconnect Express
PMC	PCI Mezzanine Card
SDK	Software Development Kit
USB	Universal Serial Bus
XMC	PCIe Mezzanine Card

Table of contents

1. Overview

This manual describes the VME-CPU/T10 and the VME-CPU/T10-F together as VME-CPU/T10, differences will be noted.
The standard version VME-CPU/T10 comes with all essential components and functionalities and is designed as replacement for the MVME5110.
The VME-CPU/T10-F is only equipped with certain components as described on page 12.

1.1 Differences between VME-CPU/T10 and VME-CPU/T10-F

The table below describes only the differences between the VME-CPU/T10 and the VME-CPU/T10-F. For further detail read the description of the boards on page 10 and 12 or chapter “Technical Data“ from page 27

	VME-CPU/T10	VME-CPU/T10-F
Processor	QorIQ® T1022	QorIQ T1014
Number of CPU-cores	2	1
NV-RAM	512kByte – MRAM serial 512kByte – MRAM parallel	512kByte – MRAM parallel
RTC	Epson RX8035 – Battery	None
Serial interfaces	1 x RS232 / FP (Rx/Tx/Cts/Rts only) Additionally optional: 1 x RS232 / P2	1 x RS232 / FP (Rx/Tx/Cts/Rts only)
PMC slot	2 x 32Bit	---
XMC slot	2 x 1 Lane (alternative to PMC slot)	---
PMC-IO	P4V2-64ac / P4V2-46dz	No
Power consumption	< 15W typ	< 10W typ

1.2 VME-CPU/T10 Standard Version

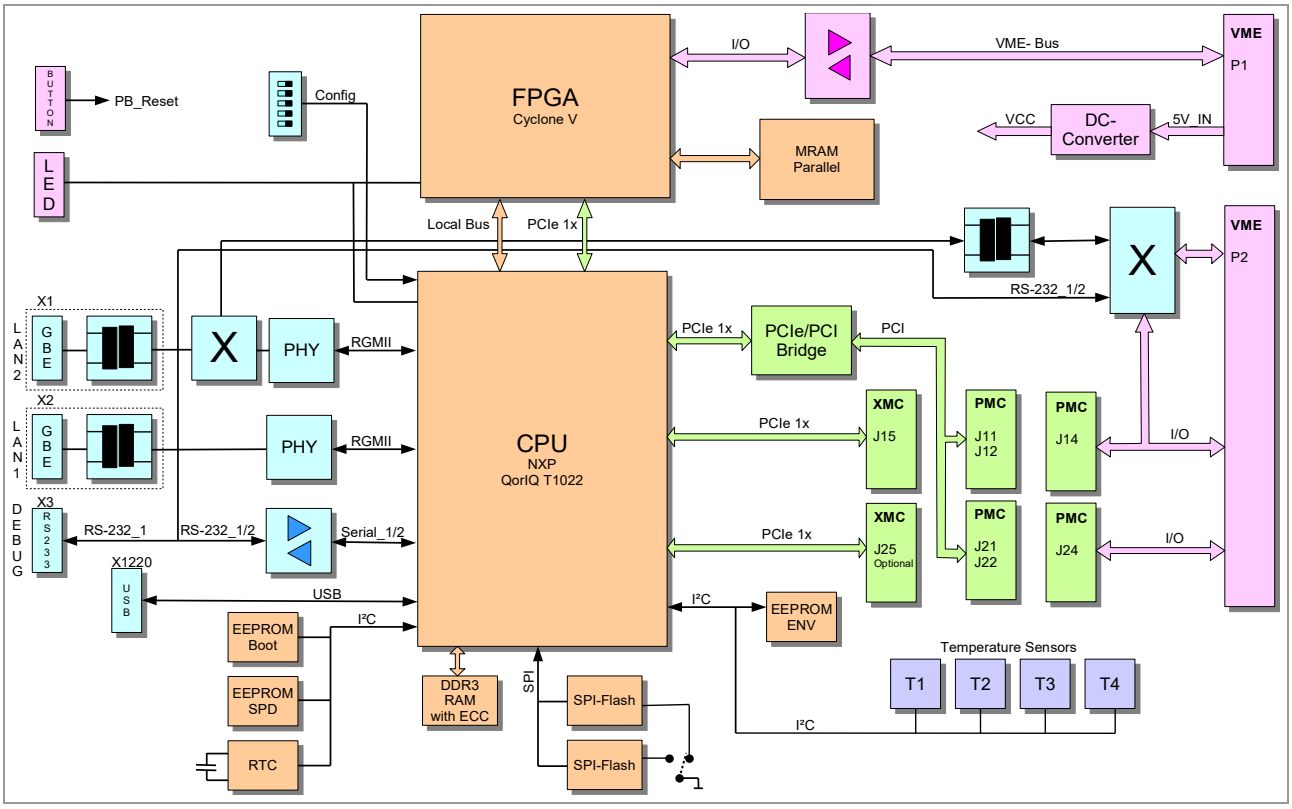


Figure 1: Block circuit diagram of VME-CPU/T10

The VME-CPU/T10 is a 64-Bit VME PowerPC™ Master CPU board with 2 XMC/PMC slots. The NXP® PowerPC® QorIQ® T1022 with 1.2 GHz features two 64-bit e5500 Power Architecture® processor cores with high performance data path acceleration architecture (DPAA) and network peripheral interfaces.
The local memory bus is 64 bits wide plus 8 bits ECC with an overall capacity of 512 Mbyte.
16 Mbyte SPI Flash for boot loader and 32 Kbit I²C EEPROM for U-Boot environment offer non-volatile memory spaces.

The VME-CPU/T10 is equipped with a second 16 Mbyte backup SPI Flash selectable by jumper that can be used for system recovery, if a system crash occurs during a firmware update.

The Altera® Cyclone® V FPGA is connected to the CPU by local bus for low latency data exchange and by PCI Express® for high bandwidth data exchange. The VMEbus master interface offers a A16/A24, D16/D8 (EO) and an SGL arbiter. A VMEbus slave interface is not supported.

The XMC1 interface comes with 1 lane PCIe bus and the XMC2 interface with 4 lane PCIe bus. They are designed according to VITA™ 42.3.
Both PMC interfaces support 32-bit/66 MHz PCI bus according to PCI Local Bus Specification 3.0.

The VME-CPU/T10 is equipped with two Gigabit Ethernet interfaces accessible at the front panel. One of the Ethernet interfaces can be routed to VME P2 (100 Mbit/s only).

A Console (Serial) RS-232 interface is accessible via an RJ45 connector at the front panel and additionally via VME P2 connector.

The Flash memory carries the standard boot program “Das U-Boot” and enables the VME-CPU/T10 to boot various operating systems from on-board Flash or network.
BSPs are available from esd as described in the “Order Information” on page 63.
The esd EtherCAT master is available for the BSPs developed by esd (see page 64).

Customization of the VME-CPU/T10 is available on request:
Customized options are available for customized serial production in reasonable quantities. Please contact our sales team for detailed information.
For example...

- CPU Type
The VME-CPU/T10 is also available with the power saving single core QorIQ CPU T1014 with 1 lane PCIe (therefore only one XMC interface) on request.

- Memory
The memory can be extended with larger MRAM, DDR3 RAM and Flash. An additional serial MRAM is also available. Instead of the battery a Gold Cap can be equipped.

- Extended Temperature Range
If an extended temperature range is requested please ask for the -40 °C … +70 °C version of the VME-CPU/T10.

- Special P0 Pin Routing
A special P0 pin routing according to VITA 35 P4V0-64 or customized routings, e.g. Ethernet, serial or PMC Slot2 J4 are available on request.

- Health Controller
On request a health controller is available for monitoring of the board's status, as voltages, temperature, board type. Additionally a watchdog can be used.

1.3 Version VME-CPU/T10-F

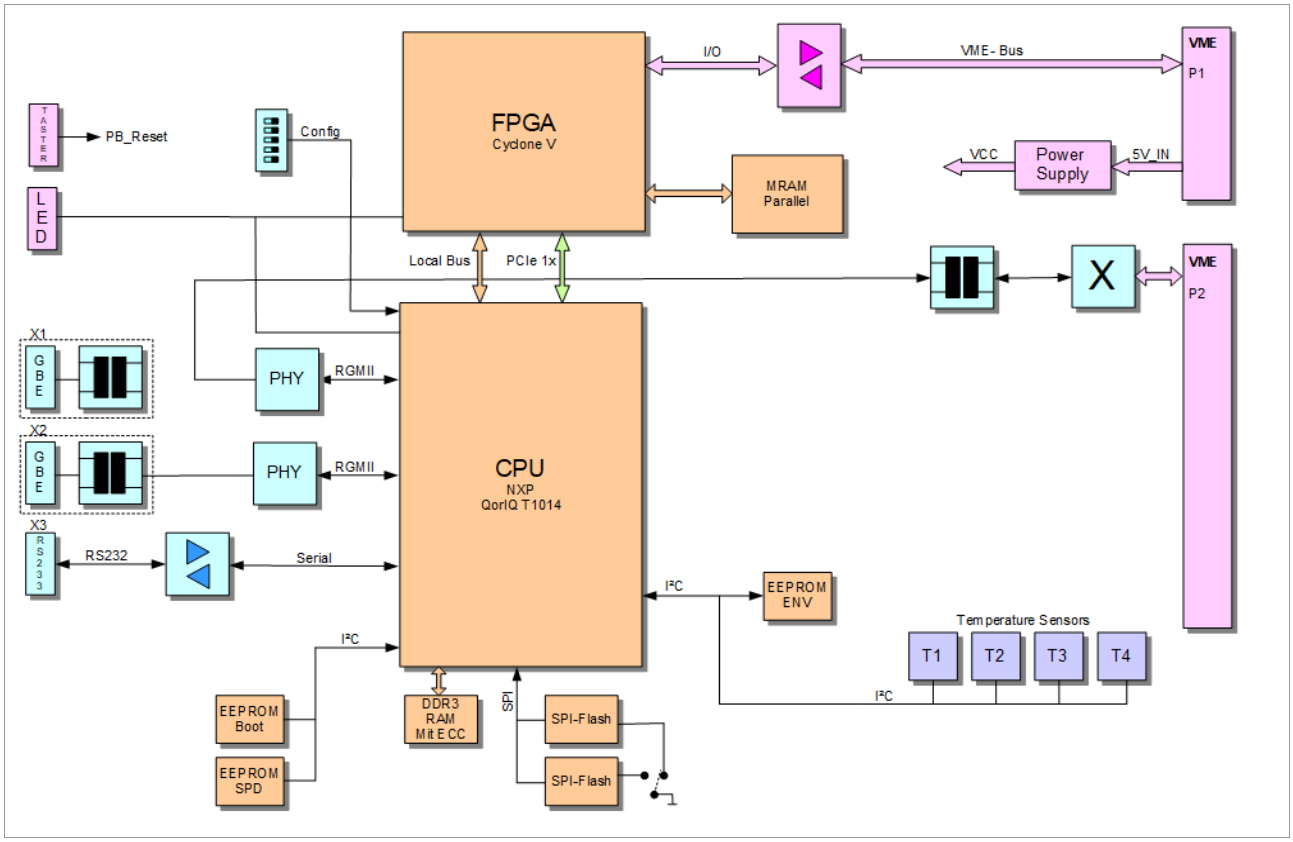


Figure 2: Block circuit diagram of VME-CPU/T10-F

The NXP® PowerPC® QorIQ® T1014 with 1.2 GHz features a 64-bit e5500 Power Architecture® processor core with high performance data path acceleration architecture (DPAA) and network peripheral interfaces.
The PMC/XMC slots are not available in the VME-CPU/T10-F version.

The VME-CPU/T10-F comes with two Gigabit Ethernet interfaces. One Ethernet interface is routed to VME P2 (100 Mbit/s only) and can be routed to the front panel. The other interface is accessible at the front panel.
A Console (Serial) RS-232 interface with RJ45 connector is accessible at the front panel.

2. PCB View with Connectors

2.1 VME-CPU/T10

2.1.1 PCB Top Layer VME-CPU/T10

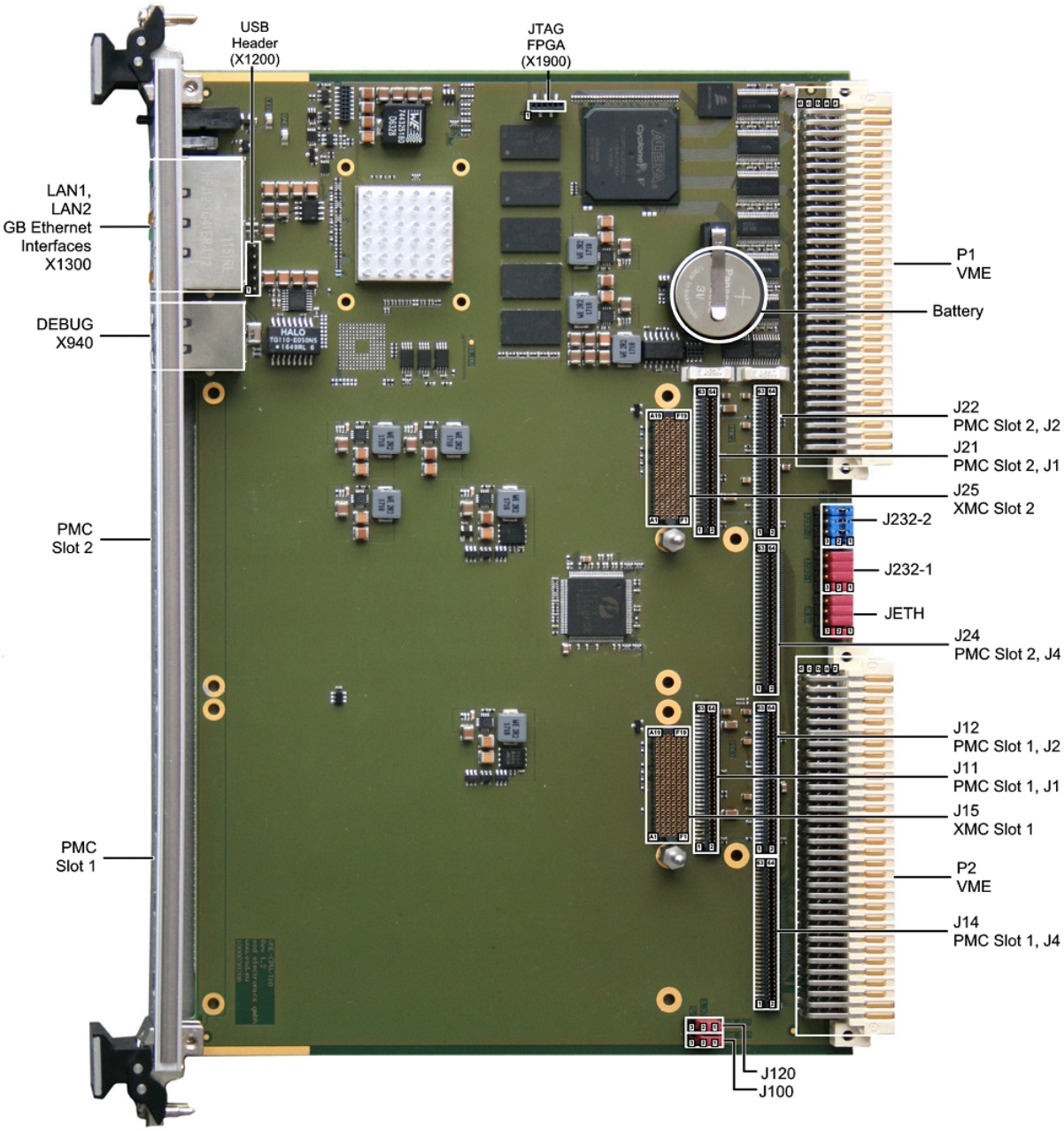


Figure 3: PCB top view VME-CPU/T10

NOTICE
Read chapter “Hardware Installation” on page 24 before starting the installation of the hardware!

See also from page 34 for signal assignment of the connectors.
The JTAG connector (X400) and the CPU Debug connector (X900) have to be connected on the PCB bottom side of the VME-CPU/T10 (see Figure 4 for the position of the connectors and pins).

2.1.2 PCB Bottom Layer View with Coding Switches VME-CPU/T10

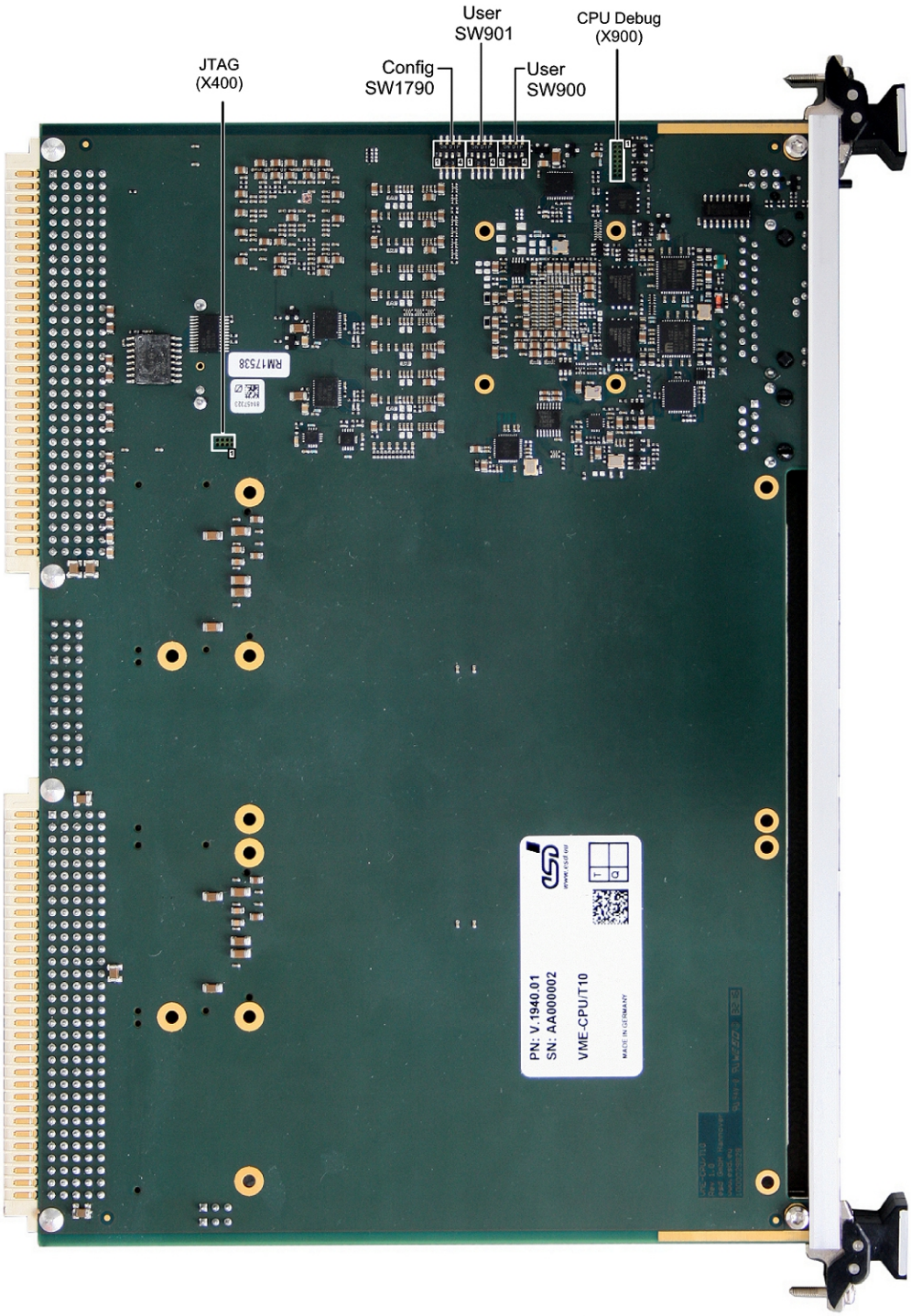


Figure 4: PCB bottom view VME-CPU/T10

See also from page 34 for signal assignments of the connectors.
esd offers special adapters as accessories, see “Order Information” on page 63.

The coding switches are described on page 20.

2.2 VME-CPU/T10-F

2.2.1 PCB Top Layer VME-CPU/T10-F

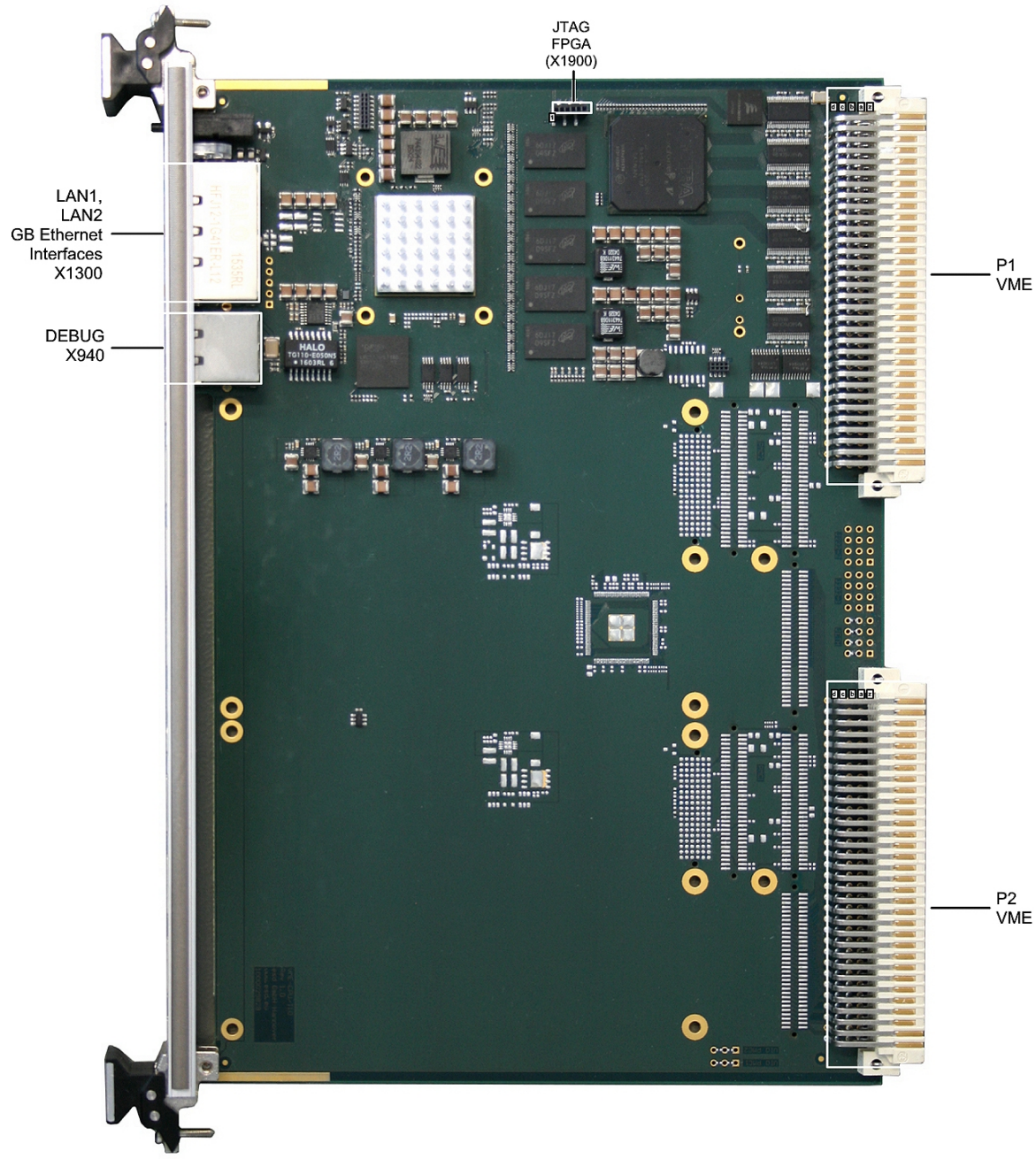


Figure 5: PCB top view VME-CPU/T10-F

NOTICE
Read chapter “Installation” on page 24 before starting the installation of the hardware!

See also from page 34 for signal assignment of the connectors.
The CPU Debug connector (X900) has to be connected on the PCB bottom side of the VME-CPU/T10-F (see Figure 6 for the position of the connectors and pins).

2.2.2 PCB Bottom Layer View with Coding Switches VME-CPU/T10-F

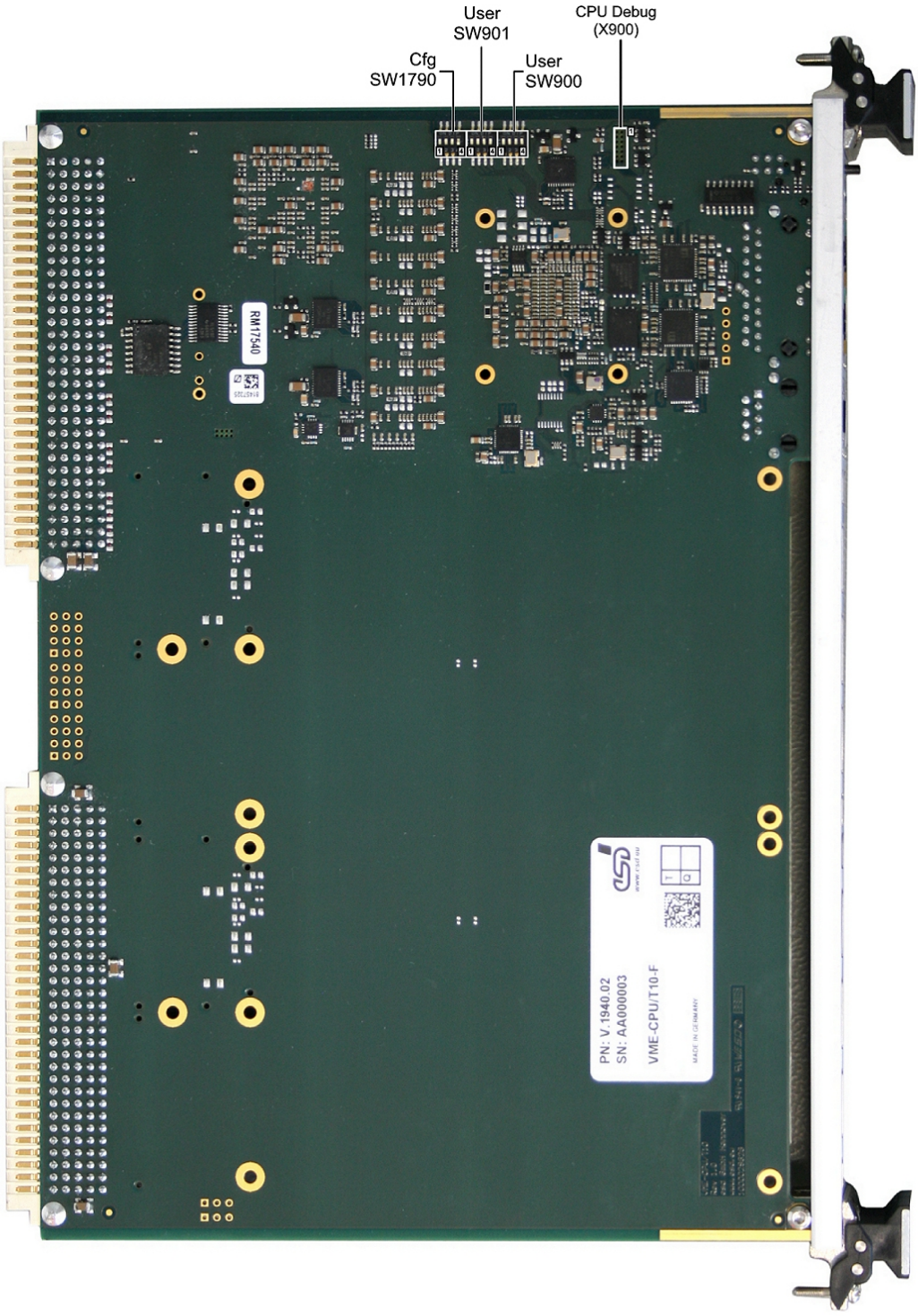


Figure 6: PCB bottom view VME-CPU/T10-F

See also from page 34 for signal assignments of the connectors.
esd offers special adapters as accessories, see “Order Information” on page 63.

The coding switches are described on page 20.

2.3 Front Panel

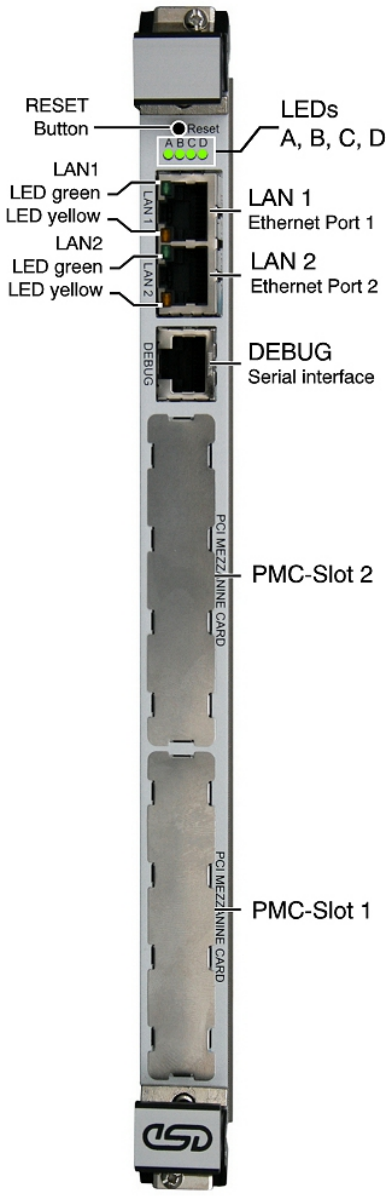


Figure 7: Connectors and LEDs VME-CPU/T10

The PMC interfaces are not available on the VME-CPU/T10-F version.

2.3.1 Reset

In the front panel a reset button is accessible, which is managed by dedicated hardware. Here a debouncing of the signal is made.

- Push the button for at least 1 sec for a reset of the system.

The function of the Reset button can be disabled by software configuration.

2.3.2 LED Indication of the BiColor LEDs A, B, C, D

Four BiColor LEDs are equipped in the front panel.

LED	Indicator State	Description	Signal name in schematic diagram
A	Green ON	CPU_OK	LED1940
	Red ON	FPGA not booted / CPU in Reset	
	Red Flash	tbd.	
B	Green Flash	VME_Access	LED1942
	Red Flash	VME_Access_Error occurred	
C	Green ON	No-Fail	LED1944
	Red ON	SYSFAIL	
	Red Flash	e.g.: VME_Irq pending	
D	User-defined		LED1946

Table 1: LEDs A - D

2.3.3 LED Indication of the Ethernet LEDs

The Activity and Link/Speed LEDs are integrated in the RJ45 sockets of LAN1 and LAN2.

LED	Colour	Function	Indicator State	Description
A	green	Activity	Flickering	Ethernet activity (reception and transmission of Ethernet data)
L	yellow	Link/Speed	ON	Ethernet link is established, Ethernet bit rate: 10/100/1000 Mbit/s

Table 2: Description of Ethernet LEDs

INFORMATION
If LAN 2 is routed to VME P2, the LEDs in the RJ45 socket of LAN 2 retain their function.

2.3.4 PMC / XMC Slots

INFORMATION
The XMC/PMC interfaces are not available in the version VME-CPU/T10-F.

In the VME-CPU/T10 standard version two slots for PMC-AddOns are provided. Both slots use a common PCI-Bus (32-bit, 33/66MHz).
The PMC-IO signals are connected to the VMEbus P2 according to „P4V2-64ac“ or „P4V2-46dz“.

Furthermore both slots can be used as XMC slots, yet the XMC IO-connectors J16/J26 are not equipped. The second XMC slot can only be used if the CPU T1022 is equipped. (Due to a reduced number of PCIe lanes of the CPU T1014).

For the generation of the 3.3V operating voltage of the PMC / XMC slots the following is provided:
a.) If the 3.3V supply voltage of the VMEbus is available, it is electronically connected to the corresponding PMC slot.
b.) If the 3.3V supply voltage of the VMEbus is not available, the 3.3V for the PMC slot are generated via a switching regulator from the 5V VME voltage. The maximum current on the 3.3V-side is 2.5A per slot.

The VIO supply is configured individually for each slot via jumpers (see page 22). The voltage keying pins (see page 23) have to be bolted to the VME-CPU/T10 board in accordance with the configured signalling voltage (3.3 V or 5 V).

NOTICE
To ensure the EC conformity of the product in the front panel the cut outs of unused PMC slots (PMC slot 1 and 2) have to be covered by the Mezzanine filler panels (see figure 7 page 17).

3. Hardware Configuration

3.1 Coding Switches

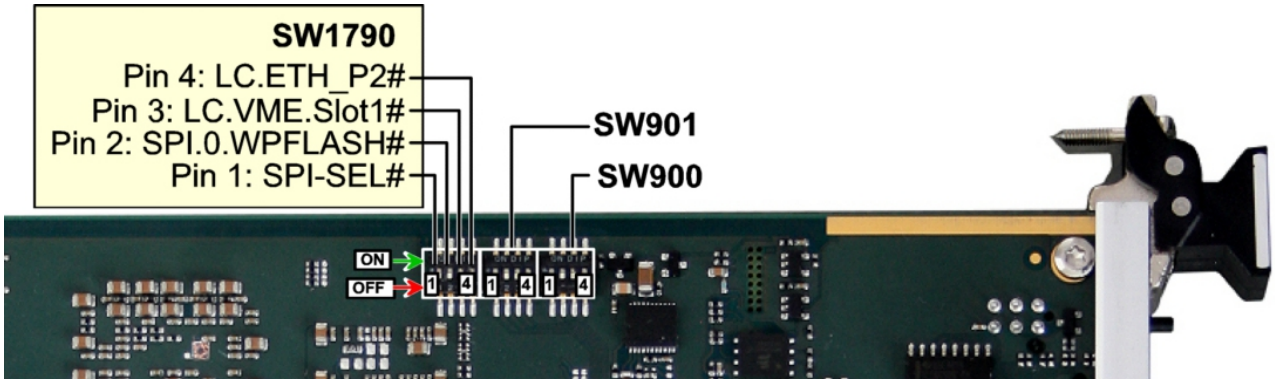


Figure 8: Coding switches on the PCB bottom layer (cut-out)

See also Figure 4 or 6 for the position of the coding switch on the board.

On delivery the DIP switches are all off.

Coding Switch	Pin	Description		
SW1790	1	SPI-SEL#	OFF	Booted from U840 flash (default)
			ON	Booted from U830 flash
	2	SPI.0.WPFLASH#	OFF	Write protection of SPI-Flash disabled (default)
			ON	Write protection SPI-Flash enabled
	3	LC.VME.SLOT1#	OFF	VME-CPU/T10 is not inserted in VME Slot 1 (default)
			ON	VME-CPU/T10 is inserted in VME Slot 1
	4	LC.ETH_P2#	OFF	Ethernet signals of LAN2 are routed to the front panel (default)
			ON	The Ethernet signals of LAN2 are routed to JETH. Note: Jumper JETH must be set accordingly to route the signals to pins (1c,2c,3c,4c) on P2 (see page 21)
SW901	1	LC_IO23	User-defined via FPGA and driver	
	2	LC_IO22		
	3	LC_IO21		
	4	LC_IO20		
SW900	1	LC_IO15	User-defined via FPGA and driver	
	2	LC_IO14		
	3	LC_IO13		
	4	LC_IO12		

Table 3: Coding Switch SW1790, SW901, SW900

3.2 Jumpers and Keying Pins

3.2.1 Jumpers J232-2, J232-1, JETH

INFORMATION
The Jumpers J232-2, J232-1 and JETH are not equipped in the version VME-CPU/T10-F. In this version the Ethernet signals are routed to the P2 pins (1c,2c,3c,4c) per default (hard wired position of JETH pins “2-3”).
The Jumpers J232-1 / -2 are all open.

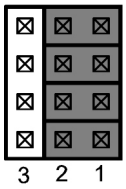
Via jumper J232 (J232-1, J232-2) an alternative assignment of four P2 signals (27c,28c,29c,30c) can be configured:
1.) The corresponding PMC-IO signals
2.) The signals of the serial interface Ser0
3.) The signals of the serial interface Ser1

Via jumper JETH an alternative assignment of four P2 signals (1c,2c,3c,4c) can be configured:
1.) The corresponding PMC-IO signals
2.) The signals of the Ethernet interface

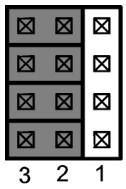
The jumpers are equipped on the PCB top layer as shown in figure 3 on page 13.

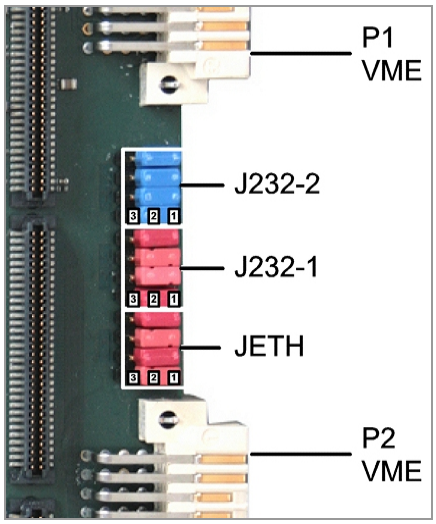
INFORMATION
All four jumper plugs of the jumpers J232-2, J232-1 and JETH have to be plugged together and in the same way.

Jumpers set on pin 1-2: (Default setting on delivery)



Jumpers set on pin 2-3:





Jumper	Jumpers set on pins	Description	P2 pins
J232-2	1 - 2	RS232 interface Ser0 (Default setting on delivery)	27c,28c, 29c,30c
	2 - 3	RS232 interface Ser1	
J232-1	1 - 2	PMC- I/O signals on P2 pins (Default setting on delivery)	
	2 - 3	RS232 signals (Ser0 or Ser1)	
JETH	1 - 2	PMC I/O-signals on P2 pins (Default setting on delivery)	1c,2c, 3c,4c
	2 - 3	ETH signals	

Table 4: Jumpers J232, JETH

Figure 9: Jumpers J232-2, J232-1 and JETH

See page 37 for the alternative assignments of P2.

3.2.2 Jumpers J100, J120

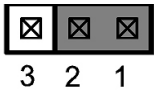
INFORMATION
Jumpers J100 and J120 are not equipped on the version VME-CPU/T10-F.

Via jumper J100 an alternative assignment of PMC-VIO (4 J11 signals on pins 19,31,45,57) can be configured:
1.) 3.3V voltage generated from 5V VME voltage (Slot 1) - Default setting on delivery
2.) 5 V VME voltage (Slot 1)

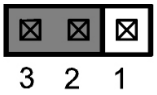
Via jumper J120 an alternative assignment of PMC-VIO (4 J21 signals on pins 19,31,45,57) can be configured:
1.) 3.3V voltage generated from 5V VME voltage (Slot 2) - Default setting on delivery
2.) 5 V VME voltage (Slot 2)

NOTICE
The I/O voltages of PMC slot 1 and slot 2 can be configured via jumper J100 and J120 to 5V or 3.3V! If the I/O voltages of one slot is set to 3.3V and of the other slot to 5V, the inserted 3.3V PMC board must be 5V tolerant to avoid damage!

The jumpers are equipped on the PCB top layer as shown in figure 3 page 13.



Jumper set on pin 1 and 2
(Default setting on delivery)



Jumper set on pin 2 and 3

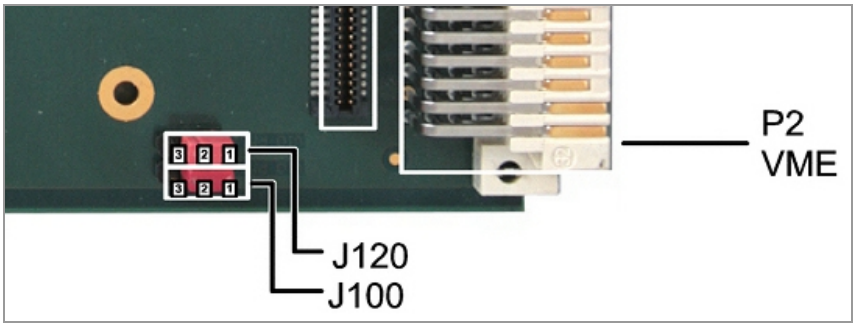


Figure 10: Jumpers J100, J120 (Default setting on delivery)

Jumper	Jumper set on pins	Description	
J120	1 - 2	3.3V power supply voltage PV I/O of J21 in slot 2 (Default setting on delivery)	**NOTICE** The PMC voltage keying pins have to be set accordingly! See page 23
	2 - 3	5V power supply voltage PV I/O of J21 in slot 2	
J100	1 - 2	3.3V power supply voltage PV I/O of J11 in slot 1 (Default setting on delivery)	
	2 - 3	5V power supply voltage PV I/O of J21 in slot 2	

Table 5: Description of jumpers J100 and J120

For the signal assignments of the connectors J11 and J21 see page 39 and 40.

3.2.3 PMC Voltage Keying Pins

INFORMATION
The voltage keying pins are not equipped on the version VME-CPU/T10-F.

The two bus signalling voltages are 3.3V and 5V. Voltage keying holes are provided for the PMC slots 1 and 2 on the VME-CPU/T10.

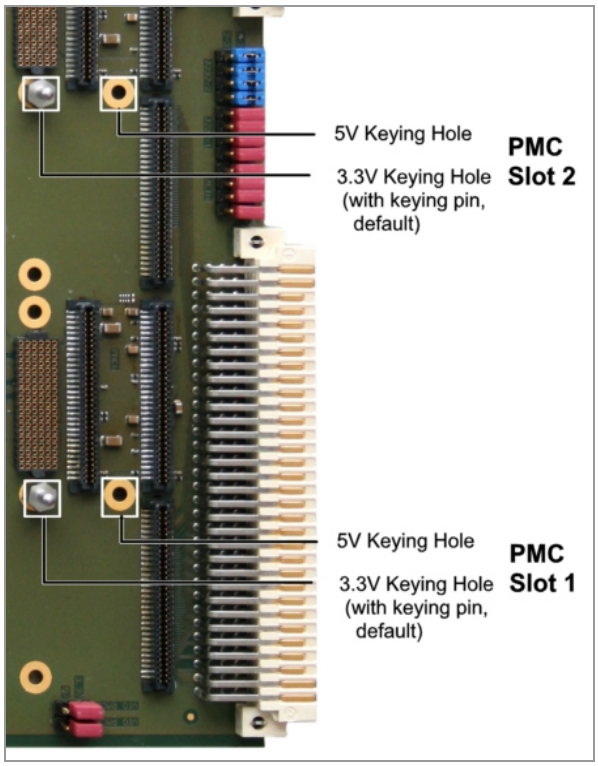


Figure 11: Keying holes (3.3V, default setting on delivery)

The voltage keying holes for the PMC slots 1 and 2 are located in the PCB as shown in figure 11.

On delivery the VME-CPU/T10 comes with the keying pins inserted in the 3.3V keying hole (default).

To change the keying of a PMC slot unscrew the keying pin and insert it in the corresponding keying hole of the PMC slot.

NOTICE
The I/O voltages (3.3V or 5V) of PMC slot 1 and slot 2 are configured via jumper J100 and J120 (see page 22). Make sure that the keying pins are inserted in accordance with the configuration of these jumpers.

4. Hardware Installation and Change of Battery

NOTICE
Read the safety instructions at the beginning of this document carefully, before you start with the hardware installation!

DANGER
Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the VME-CPU/T10 is to be integrated.
→ Disconnect all hazardous voltages (mains voltage) before opening the system.
→ Ensure the absence of voltage before starting any electrical work.

NOTICE
Electrostatic discharges may cause damage to electronic components.

→ To avoid this, discharge the static electricity from your body *before* you touch the VME-CPU/T10.
→ Furthermore, you should prevent your clothes from touching the VME-CPU/T10, because your clothes might be electrostatically charged as well.

4.1 Installation

Procedure:

1. Switch off your system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. Disconnect the system from the mains.

   DANGER
   Hazardous Voltage
   Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the VME-CPU/T10 is to be integrated.

   → Disconnect all hazardous voltages (mains voltage) before opening the system.
   → If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (i.e. with caution label).
   → Ensure the absence of voltage before starting any electrical work

4. Open the system's case if necessary.
5. Make sure that the VME-CPU/T10 is configured according to your needs:
   - For the configuration of the hardware see chapter “Coding Switches” on page 20.
   - Read chapter “Jumpers J232-2, J232-1, JETH” for the configuration of an alternate assignment of P2 signals, see page 21.
   - PMC-VIO of PMC slot 1 and 2 can be configured as 3.3V or 5V signalling voltage via Jumpers J100, J120, see page 22.
     Additionally the PMC Voltage Keying Pins have to be inserted in the corresponding 5V or 3.3V keying holes as described on page 23.
6. If you want to install XMC/PMC boards on the VME-CPU/T10, remove the Mezzanine filler panels of the cut outs of PMC slot 1 or 2 in the front panel.

NOTICE
For sufficient EMC shielding an installed XMC/PMC board should make contact to the VME-CPU/T10 nearly completely around its front panel. For this purpose mount a conductive O-ring on the front panel of your XMC/PMC board before you install it on the VME-CPU/T10. Additionally or instead of it use shielding material as for example conductive shielding gasket.

7. Carefully install the XMC/PMC boards in PMC slot 1 or 2 of the VME-CPU/T10 carrier board.

NOTICE
To ensure the EC conformity of the product the cut outs of unused PMC slots in the front panel have to be covered by the Mezzanine filler panels (see figure 7 page 17).

8. Insert the VME-CPU/T10 board into the selected VME slot. Carefully push the board until it snaps into place.
9. Fasten the mounting screws in the front panel.
10. Close the system's case again (if necessary).
11. Connect the Ethernet and the DEBUG interfaces via the connectors in the front panel of the VME-CPU/T10.
12. Connect the system to mains again (mains connector or safety fuse).
13. Switch on the system and the peripheral devices.
14. End of hardware installation.
15. Set the interface properties in your operating system. Refer to the documentation of the operating system.

4.2 Demounting

Procedure

A1. Switch off the VME system and if necessary other network participants. Disconnect the connectors in the front panel.

A2. Disconnect the system from the mains.

DANGER
Hazardous Voltage
Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages.

→ Disconnect all hazardous voltages (mains voltage) before opening the system.
→ If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (i.e. with caution label).
→ Ensure the absence of voltage before starting any electrical work

A3. Discharge your body as described above.

A4. Open the case if necessary.

A5. Unfasten the mounting screws in the front panel.

A6. Unfasten the VME-CPU/T10 by activating the eject lever and pull the module carefully out of the slot.

4.3 Change of Battery

INFORMATION
The battery is not equipped in the version VME-CPU/T10-F.

The VME-CPU/T10 comes with an RTC (Real Time Clock), which is energised with a battery. The battery is plugged in a holder directly on the board.
Battery type: BR2032, 3V.

Procedure:

1. Demount the module as described in chapter: “4.2 Demounting”.
2. Remove the old battery carefully out of the holder (see figure 3, page 13).

DANGER
Risk of personal injury due to explosion or leakage of the battery!
Improper usage of the battery such as overheating, short-circuiting or mechanical damage may cause an explosion or leakage.

→ Do not replace the battery by an incorrect type.
→ Do not recharge the battery.
→ Insert the battery properly, with the +/- terminals correctly oriented.

→ Dispose used batteries according to the national instructions.

3. Insert the new battery carefully with positive side facing up.
4. Install the module as described in chapter: “4.1 Installation”.

5. Technical Data

5.1 General Technical Data

Power supply voltage	Nominal voltage: depending on slot used: **VME interface:** 5V / I_{5V_MAX} = tbd., **XMC/PMC slots:** 3.3 V / $I_{3.3V\_MAX}$ = 3 A, Absolute maximum power (CPU): P_{+5V_MAX} = 15 W Typical power (CPU): VME-CPU/T10: P_{+5V_TYP} = 7.5 W VME-CPU/T10-F: P_{+5V_TYP} = 6 W	
Connectors	LAN1 LAN 2	RJ45 socket (X1300, Halo HFJ12-1G41ER-L12RL) - IEEE802.3, 10/100/1000 BaseT, Port 1,2
	DEBUG	RJ45 socket (X940, MOLEX 43249-8927) - Serial Debug
	P1 P2	Harting: VG160 – 0201 160 2102 - VME Harting: VG160 – 0201 160 2102 - VME
	The following connectors are only equipped on the standard version VME-CPU/T10. They are not available on the version VME-CPU/T10-F.	
	J11 J12 J14	64-pin PMC connector (TE: 5120521-1) - PMC J1, Slot 1 64-pin PMC connector (TE: 5120521-1) - PMC J2, Slot 1 64-pin PMC connector (TE: 5120521-1) - PMC J4, Slot 1
	J21 J22 J24	64-pin PMC connector (TE: 5120521-1) - PMC J1, Slot 2 64-pin PMC connector (TE: 5120521-1) - PMC J2, Slot 2 64-pin PMC connector (TE: 5120521-1) - PMC J4, Slot 2
	J15 J25	64-pin connector (Samtec: ASP-103614-04) - XMC J15, Slot 1 64-pin connector (Samtec: ASP-103614-04) - XMC J25, Slot 2
	The following connectors are only for test- and programming purposes:	
	CPU Debug	Pass-Thru micro socket (CLM108-02-F-D-BE, X900) - Debug interface of the CPU and the Health Controller
	JTAG	Pass-Thru micro socket (CLM104-02-F-D-BE, X400) - JTAG interface additionally via XMC-P11 and P12
	FPGA JTAG	Pass-Thru micro socket (RSM-106-02-T-S, X1900) - JTAG interface for FPGA
	USB	VME-CPU/T10 standard version only: USB-Header (MPE: 087-1-005-0-S-XSO-1130, X1220)
Temperature range	Operating temperature: 0 °C ... + 55 °C ambient Storage temperature: -20 °C ... + 70 °C ambient	
Humidity	0% ... 90%, non-condensing	
Dimensions	6 HP / 4 U	
Weight	Approx. 450 g	

Table 6: General data of the module

5.2 CPU and Memory

CPU	NXP QorIQ T1022 (VME-CPU/T10) or T1014 (VME-CPU/T10-F), 1.2 GHz, 64-bit, e5500 core double precision floating point unit
RAM	512MB DDR3L with ECC, 72-bit data bus, up to 800 MHz
Flash memory (NOR)	2x 16 MByte, selectable via jumper. Single Bit SPI interface, max. 50MHz bus clock 100.000 read / write cycles, >20 years data retention
NV memory	VME-CPU/T10 standard version only: 1 x 512kByte MRAM Single Bit SPI Interface, max. 40MHz bus clock 10^{14} read / write cycles, >10 years data retention The NV memory is not equipped in the VME-CPU/T10-F version!
EEPROM	1x 32 Kbit I²C EEPROM for U-Boot environment, 1x 4 Kbit RAM SPD info DDR RAM, 1x 32 Kbit EEPROM for Bootstrapping

Table 7: CPU and memory

5.3 FPGA

Type	Altera Cyclone V 5CGXFC4C7F23C8N (0°C .. 85°C)
Interface to CPU	16 Bit to enhanced Local Bus of the T1014/T1022 (100 MHz), PCI Express with one Lane, 3 Interrupts.
Configuration	The FPGA is booted via a connected Quad SPI Flash. The Flash can be programmed and updated via the CPU-SPI interface.
Function	VME Master-Interface A16/A24 D16/D8(EO), connected via PCIe

Table 8: Data of the FPGA

5.4 Ethernet Interface

Number of Ethernet interfaces	2x Gigabit Ethernet (LAN 1, LAN 2)
Standard	IEEE 802.3, 10BASE-T, 100BASE-TX, 1000BASE-T
Bit rate	10/100/1000 Mbit/s
Controller	Integrated in CPU
Connection	Twisted Pair (compatible to IEEE 802.3),
Electrical isolation	Via transformer
Connector	2x at RJ-45-socket with integrated transformer in the front panel
Special Feature	One interface is routed as 100MBit via electrical switch „TS3L4892RHHR“ and jumper to P2 (conforms with MVME5110).

Table 9: Data of the Ethernet interfaces

5.5 Serial Interfaces

Number	2 asynchronous serial interfaces
Standard	EIA/TIA-232E
Controller	Integrated in CPU
Bit rate	Value range: 9600 Baud to 115200 Baud Default setting: 115200 Baud, 8 Bit, No Parity 1 Stop-Bit
Physical Interface	RS232
Software	Standard operating system drivers
Connectors	Serial 1 (Console): RJ45 socket, assigned as MVME5110, ONLY Rx/Tx/RTS/CTS are assigned, the other connector signals are supplied with the required potential via a resistor. Serial 2: Connected to P2 via jumper

Table 10: Data of the serial interfaces

5.6 I²C Interface

Number	3
Standard	I²C-Bus Specification Rev. 6
Bit rate	100kBit, optional 400kBit
Topology	Controller integrated in CPU
Physical Interface	3,3 V, not 5V tolerant
1. I2C interface	Devices: CPU Setup EEPROM, DDR3 RAM SPD EEPROM, RTC
2. I2C interface	Devices: PCIe to PCI Bridge, Health Controller, U-Boot Env EEPROM.
3. I2C interface	Reserved

Table 11: Data of the I²C interface

5.7 Parallel MRAM

The complete MRAM can be accessed memory-mapped. The MRAM can be accessed via a register interface (as in the MVME5110), but only 64kByte can be addressed.

Number	1
Data width	8-Bit
Size	512 kByte

Table 12: Data of the Parallel MRAM

5.8 XMC Interface

INFORMATION
The XMC interface is not equipped in the version VME-CPU/T10-F.

Number	2
Standard	XMC according to VITA 42.3, 1-lane PCI EXPRESS® acc. to PCIe 1.1 (with T1022, T1042)
Lanes	XMC1: 1 lane, XMC2: 4 lanes
Mode	As device
Connector	Via XMC J15, J25

Table 13: Data of the XMC interface

5.9 PMC Interface

INFORMATION
The PMC interface is not equipped in the version VME-CPU/T10-F.

Standard	PMC according to IEEE Standard 1386-2001 and IEEE Standard 1386.1-2001
PCI bus	PCI bus according to PCI Local Bus Specification 3.0, 32 bit 33/66 MHz, PCI bus master capability
Voltage	3.3 V, (5 V tolerant)
Frequency	33/66 MHz
Mode	Non Monarch
Connector	Via J11, J12, J21, J22, J14, J 24 – Assignment according to IEEE1386

Table 14: Data of the PMC interface

5.10 Memory Interface

Number	1 SPI interface
Controller	integrated in CPU
Physical Interface	3.3 Volt, only internal on the board
Bit rate	> 25 MBit/sec
Usage	U-Boot Image for the CPU

Table 15: Data of the Memory Interface

5.11 USB, USB Host Interface

INFORMATION
The USB interface is not equipped in the version VME-CPU/T10-F.

Number	1x USB host
Standard	USB 2.0, max. 480 Mbit/s
Topology	Host Controller integrated in CPU
Max. current per port @5V	500 mA, short-circuit-protected
Electrical isolation	None
Software support	- OHCI-Host controller- and device driver - driver of the operating system
Connector	Onboard 5-pin header on the board

Table 16: Data of the USB Host interface USB

5.12 Real-Time Clock (RTC)

INFORMATION
The Real-Time Clock is not equipped in the version VME-CPU/T10-F.

Type	Epson RX8035SA
Connection	I^2C Bus
Accuracy	± 5 ppm at T_{amb} = 25 °C (< 13 s/month)
Buffer/Hold time	Battery BR2032, minimum 5 years hold time at 25°C

Table 17: Data of RTC

5.13 AC - Fail

Signalling	The VMEbus Signal ACFAIL is connected to an interrupt input of the CPU via FPGA
Action	In an interrupt-triggered routine (implementation depends on the operating system) user data are written in the MRAM. The signal can trigger an interrupt depending on the operating system.

Table 18: AC Fail data

5.14 Software Support

The flash memory carries the standard boot program “Das U-Boot” and enables the VME-CPU/T10 to boot various operating systems from network or on-board Flash, network or USB.
BSPs from esd are available as described in the Order Information on page 63

The esd EtherCAT master is available for the BSPs developed by esd (see page 64).

For detailed information about the driver availability for your operating system, please contact our sales team: sales@esd.eu

5.15 Firmware License

The complete local firmware is stored in the internal flash and can be updated as required. The VME-CPU/T10 module can be configured by serial console.

Bootloader	“Das U-Boot” (Saving / editing of variables, e.g. IP-addresses)
License information	GNU This product uses the open source-bootloader “Das U-Boot”. The U-Boot-source code is released under the terms of the GNU Public License (GPLv2+). The complete text of the license is contained in the esd-document “3rd Party Licensor Notice” as part of the product documentation. esd provides the complete bootloader-source code on request. esd strives to restore all changes on the bootloader into the official sources. The homepage of the U-Boot project is: http://www.denx.de/wiki/U-Boot.
Update Mechanism	Ethernet
System Boot	The system can be configured so that it can boot from one of the two SPI-Flash memories (selectable via jumper). Fixed system settings as MAC address and configurable settings (e.g. IP address) are stored in U-Boot variables in the EEPROM, which is connected via I²C.

6. Description of the VME Interface

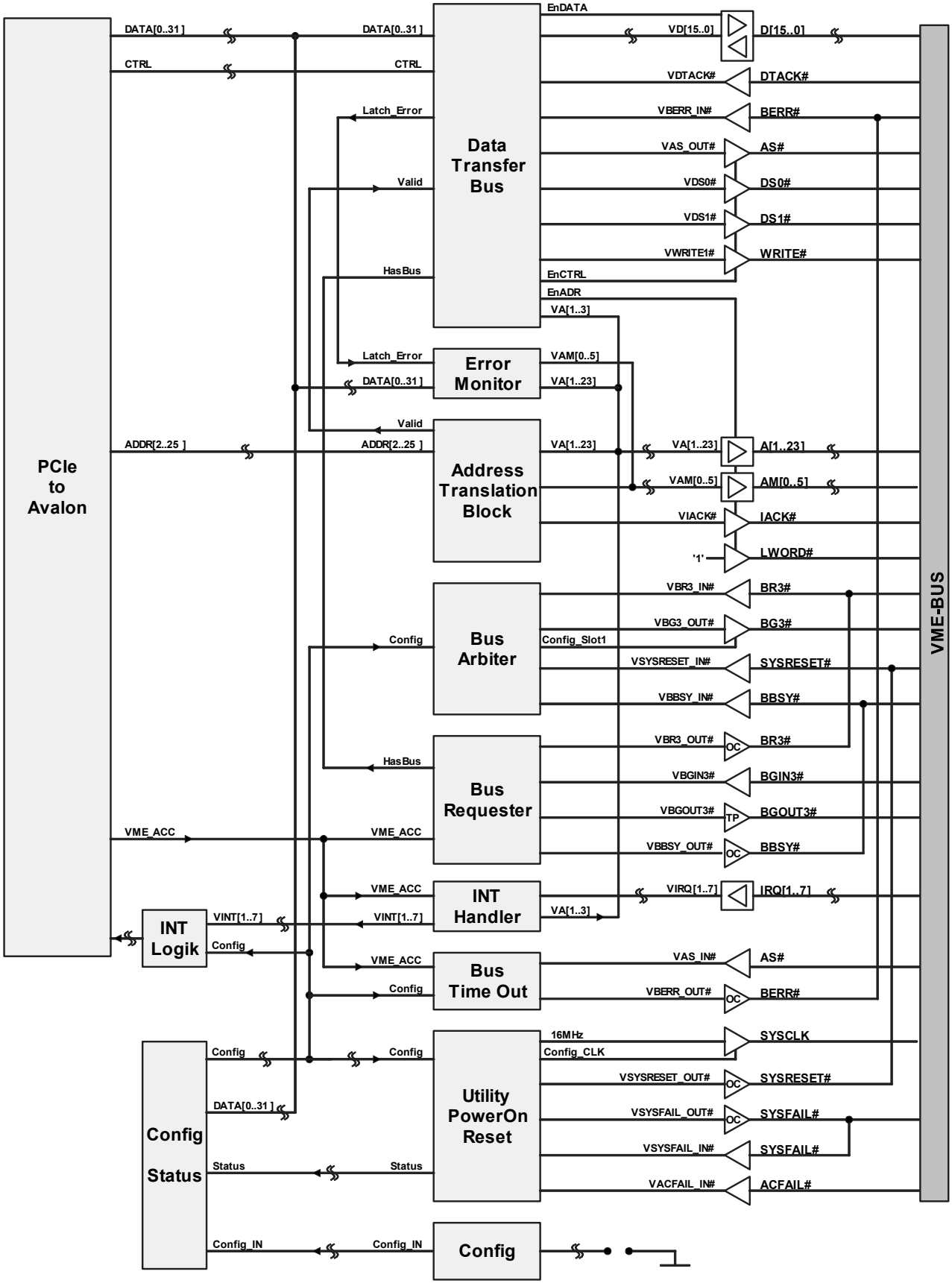


Figure 12: Block circuit diagram of VME interface

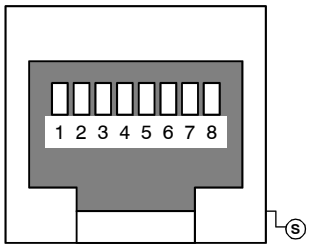
7. Connector Assignments

7.1 Ethernet 1000BASE-T (LAN1, LAN2)

Device connector: RJ45 socket, 8-pin, according to IEEE 802.3-2008, Table 'UTP MDI contact assignment'

The ports have an identical pin assignment.

Pin Position:



Pin Assignment:

Pin	Signal	Meaning
1	MDI0+ (TxD+)	Transmit Data +
2	MDI0- (TxD-)	Transmit Data -
3	MDI1+ (RxD+)	Receive Data +
4	MDI2+	
5	MDI2-	
6	MDI1- (RxD-)	Receive Data -
7	MDI3+	
8	MDI3-	

S	Shield	

Signal Description:

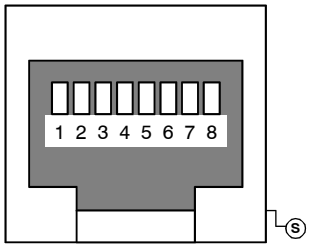
MDI0+/-, MDI0+/-, MDI1+/-, MDI1+/- ...	Ethernet data lines
Shield...	line shield connection

NOTICE
Permissible cable types: Cables of category 5e or higher have to be used to grant the function in networks with up to 1000 Mbits/s.
esd grants the EC conformity of the product if the wiring is carried out with shielded twisted pair cables of class SF/UTP or higher.

7.2 DEBUG Interface (X940)

Device connector: RJ45 socket

Pin Position:



Pin Assignment:

Pin	Signal
1	n.c.
2	RS232.0_RTS
3	GND
4	RS232.0_Tx
5	RS232.0_Rx
6	GND
7	RS232.0_CTS
8	V_{RS2320}

S	Shield

Signal Description:

n.c. ...	reserved for future applications, do not connect!
Shield...	line shield connection

7.3 VME P1 Connector

Pin	Row z	Row a	Row b	Row c	Row d
1	n.c.	D00	BBSY*	D08	n.c.
2	GND	D01	n.c.	D09	GND
3	n.c.	D02	ACFAIL*	D10	n.c.
4	GND	D03	BG0*	D11	n.c.
5	n.c.	D04	BG0*	D12	n.c.
6	GND	D05	BG1*	D13	n.c.
7	n.c.	D06	BG1*	D14	n.c.
8	GND	D07	BG2*	D15	n.c.
9	n.c.	GND	BG2*	GND	n.c.
10	GND	SYSCLK	BG3IN*	SYSFAIL*	n.c.
11	n.c.	GND	BG3OUT*	BERR*	n.c.
12	GND	DS1*	n.c.	SYSRESET*	+3.3V
13	n.c.	DS0*	n.c.	LWORD*	n.c.
14	GND	WRITE*	n.c.	AM5	+3.3V
15	n.c.	GND	BR3*	A23	n.c.
16	GND	DTACK*	AM0	A22	+3.3V
17	n.c.	GND	AM1	A21	n.c.
18	GND	AS*	AM2	A20	+3.3V
19	n.c.	GND	AM3	A19	n.c.
20	GND	IACK*	GND	A18	+3.3V
21	n.c.	IACKIN*	n.c.	A17	n.c.
22	GND	IACKOUT*	n.c.	A16	+3.3V
23	n.c.	AM4	GND	A15	n.c.
24	GND	A07	IRQ7*	A14	+3.3V
25	n.c.	A06	IRQ6*	A13	n.c.
26	GND	A05	IRQ5*	A12	+3.3V
27	n.c.	A04	IRQ4*	A11	n.c.
28	GND	A03	IRQ3*	A10	+3.3V
29	n.c.	A02	IRQ2*	A09	n.c.
30	GND	A01	IRQ1*	A08	+3.3V
31	n.c.	-12V	n.c.	+12V	GND
32	GND	+5V	+5V	+5V	n.c.

7.4 VME P2 Connector

Pin	Row z	Row a	Row b	Row c with *alternative pin-outs*			Row d
1	PMC2_IO02	PMC1_IO02	+5V	PMC1_IO01*	*ETH Rx_N*		PMC2_IO01
2	GND	PMC1_IO04	GND	PMC1_IO03*	*ETH Rx_P*		PMC2_IO03
3	PMC2_IO05	PMC1_IO06	n.c.	PMC1_IO05*	*ETH Tx_N*		PMC2_IO04
4	GND	PMC1_IO08	n.c.	PMC1_IO07*	*ETH Tx_P*		PMC2_IO06
5	PMC2_IO08	PMC1_IO10	n.c.	PMC1_IO09			PMC2_IO07
6	GND	PMC1_IO12	n.c.	PMC1_IO11			PMC2_IO09
7	PMC2_IO11	PMC1_IO14	n.c.	PMC1_IO13			PMC2_IO10
8	GND	PMC1_IO16	n.c.	PMC1_IO15			PMC2_IO12
9	PMC2_IO14	PMC1_IO18	n.c.	PMC1_IO17			PMC2_IO13
10	GND	PMC1_IO20	n.c.	PMC1_IO19			PMC2_IO15
11	PMC2_IO17	PMC1_IO22	n.c.	PMC1_IO21			PMC2_IO16
12	GND	PMC1_IO24	GND	PMC1_IO23			PMC2_IO18
13	PMC2_IO20	PMC1_IO26	+5V	PMC1_IO25			PMC2_IO19
14	GND	PMC1_IO28	n.c.	PMC1_IO27			PMC2_IO21
15	PMC2_IO23	PMC1_IO30	n.c.	PMC1_IO29			PMC2_IO22
16	GND	PMC1_IO32	n.c.	PMC1_IO31			PMC2_IO24
17	PMC2_IO26	PMC1_IO34	n.c.	PMC1_IO33			PMC2_IO25
18	GND	PMC1_IO36	n.c.	PMC1_IO35			PMC2_IO27
19	PMC2_IO29	PMC1_IO38	n.c.	PMC1_IO37			PMC2_IO28
20	GND	PMC1_IO40	n.c.	PMC1_IO39			PMC2_IO30
21	PMC2_IO32	PMC1_IO42	n.c.	PMC1_IO41			PMC2_IO31
22	GND	PMC1_IO44	GND	PMC1_IO43			PMC2_IO33
23	PMC2_IO35	PMC1_IO46	n.c.	PMC1_IO45			PMC2_IO34
24	GND	PMC1_IO48	n.c.	PMC1_IO47			PMC2_IO36
25	PMC2_IO38	PMC1_IO50	n.c.	PMC1_IO49			PMC2_IO37
26	GND	PMC1_IO52	n.c.	PMC1_IO51			PMC2_IO39
27	PMC2_IO41	PMC1_IO54	n.c.	PMC1_IO53*	*Ser0_Tx**	*Ser1_Tx**	PMC2_IO40
28	GND	PMC1_IO56	n.c.	PMC1_IO55*	*Ser0_Rx**	*Ser1_Rx**	PMC2_IO42
29	PMC2_IO44	PMC1_IO58	n.c.	PMC1_IO57*	*Ser0_RTS**	*Ser1_RTS**	PMC2_IO43
30	GND	PMC1_IO60	n.c.	PMC1_IO59*	*Ser0_CTS**	*Ser1_CTS**	PMC2_IO45
31	PMC2_IO46	PMC1_IO62	GND	PMC1_IO61			GND
32	GND	PMC1_IO64	+5V	PMC1_IO63			n.c.

n.c. ... not connected

In the version VME-CPU/T10-F the VME-P2 signals on *1c,2c,3c,4c* are assigned with the Ethernet signals! The PMC_IO signals are not connected!

Notice: The VME-P2 signals on 1c,2c,3c,4c can be assigned with Ethernet signals instead of the PMC1_IO-signals via jumper JETH!

Notice: The VME-P2 signals on 27c,28c,29c,30c can be assigned with RS-232 signals of Ser0 or Ser1 instead of the PMC1_IO-signals via Jumper J232-1 and J232-2!

7.4.1 VME-CPU/T10-P2ADA Adapters

esd offers two adapters that route the Ethernet signals on the VME P2 connector (pin *1c,2c,3c,4c*) to an Ethernet interface on an RJ45 socket. Both adapters come with the same pin assignments but the type of the P100 connector (straight/angled) and the position of the connectors on the PCB is different. See Order Information on page 63 for detail.

VME-CPU/T10-P2ADA-STRAIGHT
In this adapter version both connectors are equipped on the PCB top layer.
P100 connector: (VG96R, Harting order No.: 09 73 296 6801) with angled contacts

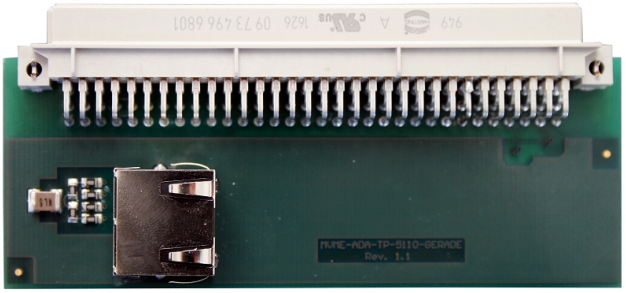


Figure 13: Top layer view (-STRAIGHT)

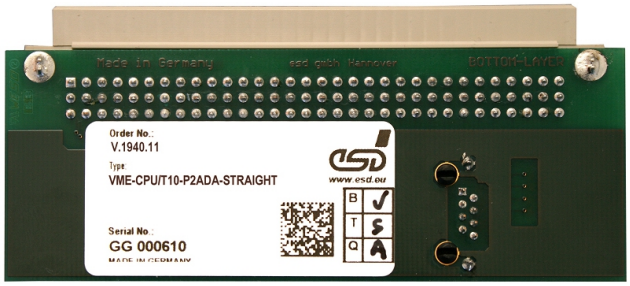


Figure 14: Bottom layer view (-STRAIGHT)

VME-CPU/T10-P2ADA-ANGLED
In this adapter version the RJ45 socket is equipped on the PCB top layer and the P100 connector is equipped on the PCB bottom layer.
P100 connector: (VG96C, Harting order No.: 09 03 296 6824) with straight contacts

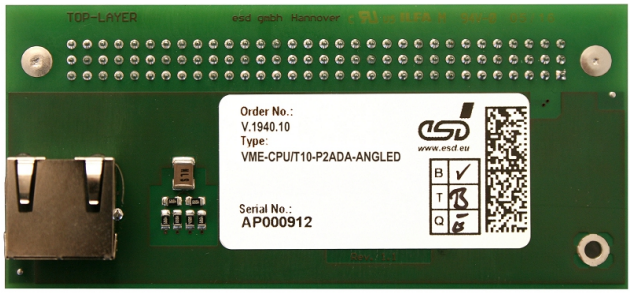


Figure 15: Top layer view (ANGLED)

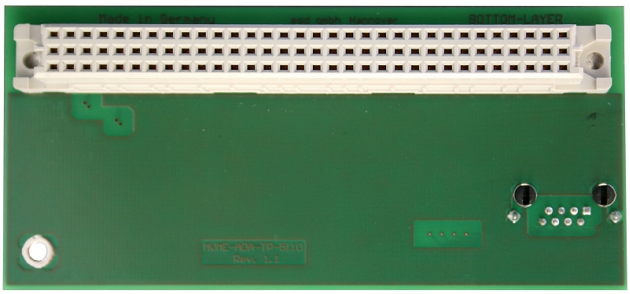


Figure 16: Bottom layer view (-ANGLED)

Pin Assignment of the RJ45 Socket:

Pin	Signal	Meaning
1	MDI0+ (TxD+)	Transmit Data +
2	MDI0- (TxD-)	Transmit Data -
3	MDI1+ (RxD+)	Receive Data +
4	Termination	
5	Termination	
6	MDI1- (RxD-)	Receive Data -
7	Termination	
8	Termination	

MDI0+/-, MDI0+/-,MDI1+/-, MDI1+/- ...	Ethernet data lines
Termination...	Termination of unused wire pairs

7.5 PMC J1-Connectors

7.5.1 PMC Connector J11 (Slot 1)

INFORMATION
The PMC interface J11 is not available in the version VME-CPU/T10-F.

NOTICE
The I/O voltages of PMC slot 1 and slot 2 can be configured via jumper J100 and J120 to 5V or 3.3V! If the I/O voltages of one slot is set to 3.3V and of the other slot to 5V, the inserted 3.3V PMC board must be 5V tolerant to avoid damage!

Pin	Signal	Signal	Pin
1	TCK	PX -12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	PRESENT#	+5V	8
9	INTD#	n.c.	10
11	GND	n.c.	12
13	PCI-CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	P_VIO1	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE3#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	PVIO_1	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	n.c. (pull-up)	n.c. (pull-up)	42
43	PAR	GND	44
45	PVIO_1	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE0#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	PVIO_1	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	n.c. (pull-up)	64

PVIO_1... The PVIO_1 voltage can be changed to 3.3 V or 5 V by jumper J100, see chapter “Jumpers J100, J120” on page 22.

7.5.2 PMC Connector J21 (Slot 2)

INFORMATION
The PMC interface J21 is not available in the version VME-CPU/T10-F.

NOTICE
The I/O voltages of PMC slot 1 and slot 2 can be configured via jumper J100 and J120 to 5V or 3.3V! If the I/O voltages of one slot is set to 3.3V and of the other slot to 5V, the inserted 3.3V PMC board must be 5V tolerant to avoid damage!

Pin	Signal	Signal	Pin
1	n.c.	PX -12V	2
3	GND	INTB#	4
5	INTC#	INTD#	6
7	PRESENT#	+5V	8
9	INTA#	n.c.	10
11	GND	n.c.	12
13	PCI-CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	PVIO_2	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE3#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	PVIO_2	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	n.c. (pull-up)	n.c. (pull-up)	42
43	PAR	GND	44
45	PVIO_2	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE0#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	PVIO_2	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	n.c. (pull-up)	64

PVIO_2... The PVIO_2 voltage can be changed to 3.3 V or 5 V by jumper J120, see chapter “Jumpers J100, J120” on page 22.

7.6 PMC J2-Connectors

7.6.1 PMC Connector J12 (Slot 1)

INFORMATION
The PMC interface J12 is not available in the version VME-CPU/T10-F.

Pin	Signal	Signal	Pin
1	PX +12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	n.c.	8
9	n.c.	n.c.	10
11	n.c. (pull-up)	PX +3.3V_1	12
13	PCI-RST#	n.c. (pull-down)	14
15	PX +3.3V_1	n.c. (pull-down)	16
17	PME#	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	PX +3.3V_1	24
25	IDSEL_AD16	AD[23]	26
27	PX +3.3V_1	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE2#	32
33	GND	n.c.	34
35	TRDY#	PX +3.3V_1	36
37	GND	STOP#	38
39	PERR#	GND	40
41	PX +3.3V_1	SERR#	42
43	C/BE1#	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	PX +3.3V_1	50
51	AD[07]	n.c.	52
53	PX +3.3V_1	n.c.	54
55	n.c.	GND	56
57	n.c.	EREADY	58
59	GND	n.c.	60
61	n.c. (pull-up)	PX +3.3V_1	62
63	GND	n.c. (pull-up)	64

7.6.2 PMC Connector J22 (Slot 2)

INFORMATION
The PMC interface J22 is not available in the version VME-CPU/T10-F.

Pin	Signal	Signal	Pin
1	PX +12V	n.c.	2
3	n.c.	n.c.	4
5	n.c.	GND	6
7	GND	n.c.	8
9	n.c.	n.c.	10
11	n.c. (pull-up)	PX +3.3V_2	12
13	PCI-RST#	n.c. (pull-down)	14
15	PX +3.3V_2	n.c. (pull-down)	16
17	PME#	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	PX +3.3V_2	24
25	IDSEL_AD17	AD[23]	26
27	PX +3.3V_2	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE2#	32
33	GND	n.c.	34
35	TRDY#	PX +3.3V_2	36
37	GND	STOP#	38
39	PERR#	GND	40
41	PX +3.3V_2	SERR#	42
43	C/BE1#	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	PX +3.3V_2	50
51	AD[07]	n.c.	52
53	PX +3.3V_2	n.c.	54
55	n.c.	GND	56
57	n.c.	EREADY	58
59	GND	n.c.	60
61	n.c. (pull-up)	PX +3.3V_2	62
63	GND	n.c. (pull-up)	64

7.6.3 PMC J4 IO Connectors

7.6.4 PMC I/O Connector J14 (Slot 1)

INFORMATION
The PMC interface J14 is not available in the version VME-CPU/T10-F.

The pin-out of J14 conforms with **„P4V2-64ac“** according to ANSI/VITA 35-2000 (R2005).

Pin	VME P2	Signal		VME P2	Pin
1	1c	PMC1_IO01	PMC1_IO02	1a	2
3	2c	PMC1_IO03	PMC1_IO04	2a	4
5	3c	PMC1_IO05	PMC1_IO06	3a	6
7	4c	PMC1_IO07	PMC1_IO08	4a	8
9	5c	PMC1_IO09	PMC1_IO10	5a	10
11	6c	PMC1_IO11	PMC1_IO12	6a	12
13	7c	PMC1_IO13	PMC1_IO14	7a	14
15	8c	PMC1_IO15	PMC1_IO16	8a	16
17	9c	PMC1_IO17	PMC1_IO18	9a	18
19	10c	PMC1_IO19	PMC1_IO20	10a	20
21	11c	PMC1_IO21	PMC1_IO22	11a	22
23	12c	PMC1_IO23	PMC1_IO24	12a	24
25	13c	PMC1_IO25	PMC1_IO26	13a	26
27	14c	PMC1_IO27	PMC1_IO28	14a	28
29	15c	PMC1_IO29	PMC1_IO30	15a	30
31	16c	PMC1_IO31	PMC1_IO32	16a	32
33	17c	PMC1_IO33	PMC1_IO34	17a	34
35	18c	PMC1_IO35	PMC1_IO36	18a	36
37	19c	PMC1_IO37	PMC1_IO38	19a	38
39	20c	PMC1_IO39	PMC1_IO40	20a	40
41	21c	PMC1_IO41	PMC1_IO42	21a	42
43	22c	PMC1_IO43	PMC1_IO44	22a	44
45	23c	PMC1_IO45	PMC1_IO46	23a	46
47	24c	PMC1_IO47	PMC1_IO48	24a	48
49	25c	PMC1_IO49	PMC1_IO50	25a	50
51	26c	PMC1_IO51	PMC1_IO52	26a	52
53	27c	PMC1_IO53*	PMC1_IO54	27a	54
55	28c	PMC1_IO55*	PMC1_IO56	28a	56
57	29c	PMC1_IO57*	PMC1_IO58	29a	58
59	30c	PMC1_IO59*	PMC1_IO60	30a	60
61	31c	PMC1_IO61	PMC1_IO62	31a	62
63	32c	PMC1_IO63	PMC1_IO64	32a	64

Notice: The signals PMC_IO53/55/57/59 are not connected to the VME P2 connector if serial signals are set via jumper J232!

7.6.5 PMC I/O Connector J24 (Slot 2)

INFORMATION
The PMC interface J24 is not available in the version VME-CPU/T10-F.

The pin-out of the J24 I/O connector conforms with **„P4V2-46dz“** according to ANSI/VITA 35-2000 (R2005).

Pin	VME P2	Signal		VME P2	Pin
1	1d	PMC2_IO01	PMC2_IO02	1z	2
3	2d	PMC2_IO03	PMC2_IO04	3d	4
5	3z	PMC2_IO05	PMC2_IO06	4d	6
7	5d	PMC2_IO07	PMC2_IO08	5z	8
9	6d	PMC2_IO09	PMC2_IO10	7d	10
11	7z	PMC2_IO11	PMC2_IO12	8d	12
13	9d	PMC2_IO13	PMC2_IO14	9z	14
15	10d	PMC2_IO15	PMC2_IO16	11d	16
17	11z	PMC2_IO17	PMC2_IO18	12d	18
19	13d	PMC2_IO19	PMC2_IO20	13z	20
21	14d	PMC2_IO21	PMC2_IO22	15d	22
23	15z	PMC2_IO23	PMC2_IO24	16d	24
25	17d	PMC2_IO25	PMC2_IO26	17z	26
27	18d	PMC2_IO27	PMC2_IO28	19d	28
29	19z	PMC2_IO29	PMC2_IO30	20d	30
31	21d	PMC2_IO31	PMC2_IO32	21z	32
33	22d	PMC2_IO33	PMC2_IO34	23d	34
35	23z	PMC2_IO35	PMC2_IO36	24d	36
37	25d	PMC2_IO37	PMC2_IO38	25z	38
39	26d	PMC2_IO39	PMC2_IO40	27d	40
41	27z	PMC2_IO41	PMC2_IO42	28d	42
43	29d	PMC2_IO43	PMC2_IO44	29z	44
45	30d	PMC2_IO45	PMC2_IO46	31z	46
47	n.c.	n.c.	n.c.	n.c.	48
49	n.c.	n.c.	n.c.	n.c.	50
51	n.c.	n.c.	n.c.	n.c.	52
53	n.c.	n.c.	n.c.	n.c.	54
55	n.c.	n.c.	n.c.	n.c.	56
57	n.c.	n.c.	n.c.	n.c.	58
59	n.c.	n.c.	n.c.	n.c.	60
61	n.c.	n.c.	n.c.	n.c.	62
63	n.c.	n.c.	n.c.	n.c.	64

7.7 XMC J5 I/O Connectors

7.7.1 XMC - J15

INFORMATION
The XMC interface J15 is not available in the version VME-CPU/T10-F.

Signal / PIN Row A		Signal / PIN Row B		Signal / PIN Row C		Signal / PIN Row D		Signal / PIN Row E		Signal / PIN Row F	
PCIe_Rx_L6p	1	PCIe_Rx_L6n	1	PX1 3.3V	1	n.c.	1	n.c.	1	VME 5V	1
GND	2	GND	2	PX1 3.3V pull-up	2	GND	2	GND	2	PCIe_RST_IN#	2
n.c.	3	n.c.	3	PX1 3.3V	3	n.c.	3	n.c.	3	VME 5V	3
GND	4	GND	4	PX1 3.3V pull-up	4	GND	4	GND	4	n.c.	4
n.c.	5	n.c.	5	PX1 3.3V	5	n.c.	5	n.c.	5	VME 5V	5
GND	6	GND	6	PX1 3.3V pull-up	6	GND	6	GND	6	PX +12V	6
n.c.	7	n.c.	7	PX1 3.3V	7	n.c.	7	n.c.	7	VME 5V	7
GND	8	GND	8	PX1 3.3V pull-up	8	GND	8	GND	8	PX -12V	8
n.c.	9	n.c.	9	n.c.	9	n.c.	9	n.c.	9	VME 5V	9
GND	10	GND	10	PX1 3.3V pull-up	10	GND	10	GND	10	GND	10
PCIe_Tx_L6p	11	PCIe_Tx_L6n	11	PX1 3.3V pull-up	11	n.c.	11	n.c.	11	VME 5V	11
GND	12	GND	12	GND	12	GND	12	GND	12	MPSENT0#	12
n.c.	13	n.c.	13	n.c.	13	n.c.	13	n.c	13	VME 5V	13
GND	14	GND	14	GND	14	GND	14	GND	14	I²C_SDA	14
n.c.	15	n.c.	15	n.c.	15	n.c.	15	n.c.	15	VME 5V	15
GND	16	GND	16	I²C_WE	16	GND	16	GND	16	I²C_SCL	16
n.c.	17	n.c.	17	n.c.	17	n.c.	17	n.c.	17	n.c.	17
GND	18	GND	18	n.c.	18	GND	18	GND	18	n.c.	18
REFCLK_4p	19	REFCLK_4n	19	n.c.	19	WAKE#	19	n.c.	19	n.c.	19

7.7.2 XMC - J25

INFORMATION
The XMC interface J25 is not available in the version VME-CPU/T10-F.

Signal / PIN Row A		Signal / PIN Row B		Signal / PIN Row C		Signal / PIN Row D		Signal / PIN Row E		Signal / PIN Row F	
PCIe_Rx_L0p	1	PCIe_Rx_L0n	1	PX2 3.3V	1	PCIe_Rx_L1p	1	PCIe_Rx_L1n	1	VME 5V	1
GND	2	GND	2	PX2 3.3V pull-up	2	GND	2	GND	2	PCIe_RST_IN#	2
PCIe_Tx_L2p	3	PCIe_Tx_L2n	3	PX2 3.3V	3	PCIe_Rx_L3p	3	PCIe_Rx_L3n	3	VME 5V	3
GND	4	GND	4	PX2 3.3V pull-up	4	GND	4	GND	4	n.c.	4
n.c.	5	n.c.	5	PX2 3.3V	5	n.c.	5	n.c.	5	VME 5V	5
GND	6	GND	6	PX2 3.3V pull-up	6	GND	6	GND	6	PX 12V	6
n.c.	7	n.c.	7	PX2 3.3V	7	n.c.	7	n.c.	7	VME 5V	7
GND	8	GND	8	PX2 3.3V pull-up	8	GND	8	GND	8	PX -12V	8
n.c.	9	n.c.	9	n.c.	9	n.c.	9	n.c.	9	VME 5V	9
GND	10	GND	10	PX2 3.3V pull-up	10	GND	10	GND	10	GND	10
PCIe_Tx_L0p	11	PCIe_Tx_L0n	11	PX2 3.3V pull-up	11	PCIe_Tx_L1p	11	PCIe_Tx_L1n	11	VME 5V	11
GND	12	GND	12	GND	12	GND	12	GND	12	MPESENT1#	12
PCIe_Tx_L2p	13	PCIe_Tx_L2n	13	n.c.	13	PCIe_Tx_L3p	13	PCIe_Tx_L3n	13	VME 5V	13
GND	14	GND	14	PX2 3.3V	14	GND	14	GND	14	I²C_SDA	14
n.c.	15	n.c.	15	n.c.	15	n.c.	15	n.c.	15	VME 5V	15
GND	16	GND	16	I²C_WE	16	GND	16	GND	16	I²C_SCL	16
n.c.	17	n.c.	17	n.c.	17	n.c.	17	n.c.	17	n.c.	17
GND	18	GND	18	n.c.	18	GND	18	GND	18	n.c.	18
REFCLK_5p	19	REFCLK_5n	19	n.c.	19	WAKE#	19	n.c.	19	n.c.	19

7.8 JTAG X900

The JTAG interface has to be connected from the bottom side of the VME-CPU/T10. esd offers an adapter, the XMC-CPU-ADAPTER-BDI as accessories. See Order Information on page 63 for more details.

7.8.1 XMC-CPU-ADAPTER-BDI

The XMC-CPU-ADAPTER-BDI (esd order No.: V.2029.02) is an interface to connect the Abatron BDI2000 or BDI3000 debugger to the VME-CPU/T10 connector X900.

Samtec CLM (16 pins) <-> box header (16 pins)

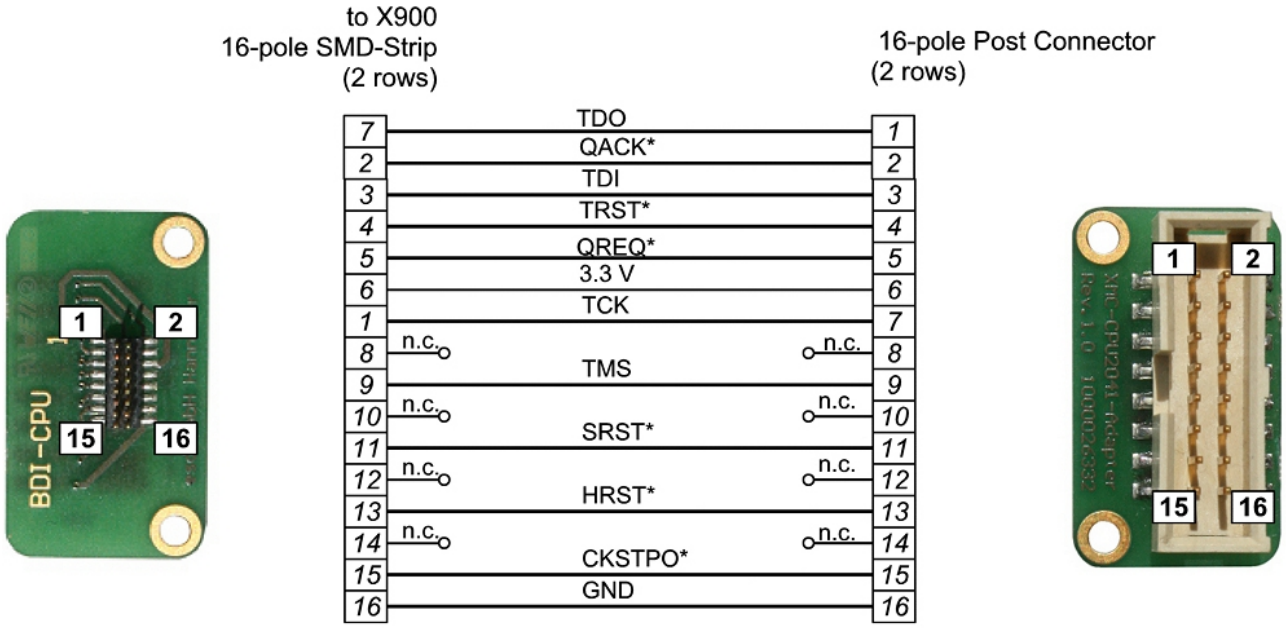


Figure 17: XMC-CPU-ADAPTER-BDI

NOTICE
The 16-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 4 on page 14 for the position of the X900 connector pins.

7.9 Debug Interface X400

INFORMATION
The connector X400 is not available in the version VME-CPU/T10-F.

The Debug interface has to be connected from the bottom side of the VME-CPU/T10.

Signal	Pin	Pin	Signal
JTAG_TDI	2	1	3.3V
JTAG_TCK	4	3	JTAG_TDO
GND	6	5	JTAG_TMS
NXP.RST#	8	7	JTAG_TRST#

NOTICE
The 8-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 4 on page 14 for the position of the X400 connector pins.

7.10 and JTAG FPGA Interface X1900

INFORMATION
The connector X1900 is not available in the version VME-CPU/T10-F.

The JTAG FPGA interface has to be connected from the top side of the VME-CPU/T10.

Pin	Signal
1	3.3V
2	FPGA_TDI
3	FPGA_TDO
4	FPGA-TCK
5	FPGA_TMS
6	GND

NOTICE
The 6-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 13 for the position of the X1900 connector pins.

7.11 USB Interface on X1200

INFORMATION
The connector X1200 is not available in the version VME-CPU/T10-F.

The JTAG FPGA interface has to be connected from the top side of the VME-CPU/T10.

Pin	Signal
1	U1_VBus
2	U1_D-
3	U1_D+
4	GND
5	U1_UID

NOTICE
The 5-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 13 for the position of the X1200 connector pins.

8. CPU

The general functions of the NXP QorIQ T1022 and T014 are not described in this manual.
Further information about the CPU can for example be downloaded from the website of the manufacturer NXP: http://www.nxp.com/

The CPU is connected to the FPGA for configuration and MRAM accesses via the 16-bit local bus or for VME accesses over PCIe bus.
The following table shows the base addresses for the physical 8- and 16-bit access modes.

Base Address	Functionality
0xF FE13 3008	GPIO register (see chapter 8.1)
0xF FF20 0000	16-bit accesses local bus
0xF FF40 0000	8-bit accesses local bus

Table 19: Base address

Table 20 shows, which access mode you should use for your data access.

	your data access					
	byte (8-bit)		word (16-bit)		long word (32-bit)	
	read	write	read	write	read	write
16-bit access mode	1 access	don't use	1 access	1 access	2 accesses	2 accesses
8-bit access mode	1 access	1 access	2 accesses	2 accesses	4 accesses	4 accesses

Table 20: Data access mode

8.1 User configuration via GPIO register

Via CPU GPIO register the settings can be handled as shown in the following table.

Address	Register name	Bits					
		31 … … 20	**19 ... ... 16**	15 ... … 13	**12**	**11 … ... 8**	7 … … 0
0xFE133008	**GPIO_4**	reserved	**SW900**	reserved	**Reset Disable**	**SW901**	reserved

Table 21: CPU register GPIO_4

Description

Name	Access	Description
SW900	ro	Read back the setting of the configuration DIP switch SW900
SW901	ro	Read back the setting of the configuration DIP switch SW901
Reset Disable	rw	When set to 1, the front panel reset switch has no functionality. Default is 0.

NOTICE
Reserved values must be written with the value that is read before.

The switches are equipped on the PCB bottom layer as described on page 14 or 16.
Read chapter “Coding Switches” on page 20 for further information about the switches.

Bit	LC_IO	SW900 Pin
19	LC_IO12	4
18	LC_IO13	3
17	LC_IO14	2
16	LC_IO15	1

Bit	LC_IO	SW901 Pin
11	LC_IO20	4
10	LC_IO21	3
9	LC_IO22	2
8	LC_IO23	1

8.2 Watchdog

The watchdog is described in the manual:
“EREF: A Programmer’s Reference Manual for Freescale Embedded Processors”.
The manual can be downloaded from the NXP website.

9. VME

The VME interface is realized in the FPGA.
A full description of the general functions of the Cyclone V FPGA is not part of this manual.
Further information about the functionality of the FPGA can be downloaded from the website of the manufacturer Altera®: https://www.altera.com/

The VME Master interface A16/A24 D16/D8(EO), is connected via PCIe.
It comes with SGL-Arbiter, System-Controller and Interrupt-Handler.

9.1 Description of the VMEbus

The VMEbus is accessible via PCIe bus with:
Vendor ID: 0x12FE
Device ID: 0x5410
Base Address Bar 0

To access the VMEbus you can use six VME access windows. Table 22 shows the address offsets of the windows in PCIe address space.
The windows A16_1 and A16_2 give access to VME A16 access mode.
For VME A24 access mode use window A24E, A24Q, A24H or A24F.

You can set the address offset for A24E, A24Q and A24H according to chapter “VME Window Configuration“ (page 56) to access the full A24 space.
In all windows you are allowed to configure your address modifiers individually.

Free configurable VME Windows:

VME Access Space

Offset		VME Windows	
from	to		
+0x0000 0000	+0x0000 FFFF	A16_1	Full A16 address space
+0x0001 0000	+0x0001 FFFF	A16_2	Full A16 address space
+0x0020 0000	+0x003F FFFF	A24E	1/8 of A24 address space
+0x0040 0000	+0x007F FFFF	A24Q	1/4 of A24 address space
+0x0080 0000	+0x00FF FFFF	A24H	1/2 of A24 address space
+0x0100 0000	+0x01FF FFFF	A24F	Full A24 address space

Table 22: VME address offsets

9.2 VME Configuration

Accessible via local bus with offset 0x0

Offset	R/W	Short	Registername	Bit 15-8								Bit 7-0							
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Controller Configuration																			
0x00	R	VERSION	Version Register	REL[15...8]								STEP[7...0]							
0x02	R	CREL	Core Release Register	YEAR[15...9]								MON[8...5]			DAY[4...0]				
0x04	R	ENDN_HIGH	Endian Register High	0x8765															
0x06	R	ENDN_LOW	Endian Register Low	0x4321															
0x08	R/W	SYSCT	System Driver Control Register	res.						SW_SYSFAIL	BERR_HOLD	res.			VBTO	res.	SW_SYSRST	res.	INT_EN
0x0A	R/W*	SYSST	System Status Register	res.				BERR_OVER	ACFAIL_S	SYSFAIL_S	BERR_S*	res.						SYSCON	VOWN
0x0C	R/W	INTINHEN	Interrupt Inhibit Enable Register	res.					ACFAIL_INH_EN	SYSFAIL_INH_EN	BERR_INH_EN	VIRQ7_INH_EN	VIRQ6_INH_EN	VIRQ5_INH_EN	VIRQ4_INH_EN	VIRQ3_INH_EN	VIRQ2_INH_EN	VIRQ1_INH_EN	res.
0x0E	R/W	RETVEC	Return Value Register	RETURN VALUE WRONG [15...8] Default Value: 0x08								RETURN VALUE SPURIOUS [15...8] Default Value: 0x60							
0x10	R/W	INTENA	Interrupt Enable Register A	res.					ACFAIL_EN	SYSFAIL_EN	BERR_EN	VIRQ7_EN	VIRQ6_EN	VIRQ5_EN	VIRQ4_EN	VIRQ3_EN	VIRQ2_EN	VIRQ1_EN	res.
0x12	R/W	INTENB	Interrupt Enable Register B	res.					ACFAIL_EN	SYSFAIL_EN	BERR_EN	VIRQ7_EN	VIRQ6_EN	VIRQ5_EN	VIRQ4_EN	VIRQ3_EN	VIRQ2_EN	VIRQ1_EN	res.
0x14	R/W	INTENC	Interrupt Enable Register C	res.					ACFAIL_EN	SYSFAIL_EN	BERR_EN	VIRQ7_EN	VIRQ6_EN	VIRQ5_EN	VIRQ4_EN	VIRQ3_EN	VIRQ2_EN	VIRQ1_EN	res.
0x16	R	INTST	Interrupt Status Register	VIRQ_ACTIVE	INTC_ACTIVE	INTB_ACTIVE	INTA_ACTIVE	res.	ACFAIL_S	SYSFAIL_S	BERR_S	VIRQ7_S	VIRQ6_S	VIRQ5_S	VIRQ4_S	VIRQ3_S	VIRQ2_S	VIRQ1_S	res.
0x18	R	INTADDR	Interrupt Ack Address	res.												IRQ Address[2...0]			res.
0x1A	R/W	INTACK	Interrupt Inhibit Acknowledge	res.	ACFAIL_INH_SET	SYSFAIL_INH_SET	BERR_INH_SET	res.	ACFAIL_ACK	SYSFAIL_ACK	BERR_ACK	VIRQ7_ACK	VIRQ6_ACK	VIRQ5_ACK	VIRQ4_ACK	VIRQ3_ACK	VIRQ2_ACK	VIRQ1_ACK	res.
0x1C	R	BERROR_1	Bus Error Monitor High	DS [15...14]		VME AM [13...8]						VME Address Bits 23-16 [7...0]							
0x1E	R	BERROR_2	Bus Error Monitor Low	VME Address Bits 15-1 [15...1]															R=1/W=0
VME Window Configuration																			
0x20	R/W	A16_1	A16_1 Configuration Register	res.							EN	res.		Address Modifier[5...0]					
0x22	R/W	A16_2	A16_2 Configuration Register	res.							EN	res.		Address Modifier[5...0]					
0x24	R/W	A24E	A24 Eighth Configuration Register	res.	ADDR[23:21]			res.			EN	res.		Address Modifier[5...0]					
0x26	R/W	A24Q	A24 Quarter Configuration Register	res.	ADDR[23:22]		res.				EN	res.		Address Modifier[5...0]					
0x28	R/W	A24H	A24 Half Configuration Register	res.	ADDR[23]	res.					EN	res.		Address Modifier[5...0]					
0x2A	R/W	A24F	A24 Full Configuration Register	res.							EN	res.		Address Modifier[5...0]					
... 0x3E	res.																		

*Reset with write '1'

VBTO	Timeout
0	4 us (default)
1	16 us

Table 23: Controller and VME window configuration

9.2.1 Configuration-/Status-Register 16-Bit, Offset 0xFF20 0000

9.2.1.1 Master Configuration

Offset Register Name and Description

0x00: VERSION read_only
Contains the version of the block “VME_Control“, subdivided in REL and STEP.
Example: 0x0100 REL=1, STEP=0

0x02: CREL read_only
Contains the creation date of the block “VME_Control“, subdivided in year, month and day

0x04: ENDN_H read_only
Test register for the request of the Endianness, fixed 0x8765

0x06: ENDN_L read_only
Test register for the request of the Endianness, fixed 0x4321

0x08: SYSCT read/write
Global setting of the behaviour and of the outputs “Sysreset“ and “Sysfail“
Default: 0x0004

Bit0:	INT_EN Global release of the three interrupt signals INTA, INTB and INTC to CPU. 0: All Interrupts disabled 1: Interrupts enabled
Bit2:	SW_SYSRST Generation of the VME signal „Sysreset“ 0: Sysreset disabled 1: Sysreset enabled NOTICE: This bit is enabled after “Power_On“ and must be reset. Note that the duration must be minimum 200ms, when generating a VME-Sysreset.
Bit4:	VBTO Setting the VMEbus Timeouts 0: 4us 1: 16us
Bit8:	BERR_Hold 0: At multiple bus access errors the last address is stored in the bus monitor 1: At multiple bus access errors the first address is stored in the bus monitor
Bit9:	SW_Sysfail Generation of the VME signal “Sysfail“ 0: Sysfail disabled 1: Sysfail enabled

0x0A: SYSST read/(write)
Reads the status, clears the bus monitor

Bit0:	VOWN 0: currently no active Bus Master 1: currently active Bus-Master
Bit1:	SYSCON 0: no system controller 1: active system controller (defined by hardware)
Bit8:	BERR_S 0: no new entry in the bus monitor 1: minimum one new entry in the bus monitor NOTICE: By writing of “1“, BERR_S and BERR_OVER will be reset
Bit9:	SYSFAIL_S 0: VME-Sysfail signal inactive 1: VME-Sysfail signal active
Bit10:	ACFAIL_S 0: VME-ACfail signal inactive 1: VME-ACfail signal active
Bit11:	BERR_OVER 1: More than one bus errors occurred

0x0C: INTINHEN read/(write)
Setting the interrupt handling for the VME interrupts
0: Interrupts transparent
1: „Inhibit-Mode“ (see chapter “Inhibit-Mode”, page 57 for more information)

0x0E: RETVEC read/write
Setting of the interrupt vectors for “spurious” and “wrong”.
“wrong”: Bus error during Interrupt-Acknowledge cycle
“spurious”: No active interrupt during Interrupt-Acknowledge cycle
Default: 0x0860

0x10: INTENA read/write
0x12: INTENB read/write
0x14: INTENC read/write
Assignment of the 3 local interrupts (ACFAIL, SYSFAIL and BERR) and the 7 vector interrupts of the VMEbus to the CPU interrupt inputs INTA, INTB and INTC.
1: The corresponding signal triggers an interrupt
0: The corresponding signal has no influence

0x16: INTST read_only
Interrupt status
1: The corresponding signal is active

0x18: INTADDR read_only
The address offset of the highest-priority, non-masked VME interrupt can be read here.
0x0000 – no interrupt active
0x0002 – VME-Irq1 is active
0x0004 – VME-Irq2 is active
…...
0x000E – VME-Irq7 is active

0x1A: INTACK read/write
Status of the VME interrupt level in “Inhibit-Mode”, and the local interrupts. (see chapter “Interrupts”)

Bit7...1:	Reading:	1: The corresponding VME interrupt level is currently in status “Inhibit”
	Writing:	1: The corresponding VME interrupt level is enabled 0: No change
Bit10..8:	Reading:	1: The corresponding local interrupt is currently in status “Inhibit”
	Writing:	1: The corresponding local interrupt is enabled 0: No change
Bit14..12:	Writing:	1: The corresponding local interrupt is set to status “Inhibit” 0: No change

0x1C: BERROR_1 read_only
0x1E: BERROR_2 read_only
If a VME access is terminated with “Bus-Error”, the bit “BERR_S” is set and the accessed VME address and the corresponding address modifier are written here.

9.2.1.2 VME Window Configuration

Offset Register Name and Description
0x20..
0x2A: read/write
VME Window configuration:
Via the following entries the 6 VME ranges in the PCIe space can be parametrized.

Bit5..0:	Address-Modifier5..0 for the bus access
Bit8:	EN 0: No access 1: Access permitted
Bit14..12:	ADDR[23:21] Address offset for small A24 ranges.

Typical presetting:
0x20: 0x012D PCIe range A16_1 configured as “Short Supervisory Access”
0x2A: 0x013D PCIe range A24F configured as “Standard Supervisory Data Access”

9.3 VME Interrupts

9.3.1 Assignment of the Interrupts

The Interrupts INTA..C are „active_low“ and assigned to the CPU interrupts as follows:

INTA <> IRQ10
INTB <> IRQ11
INTC <> IRQ01

9.3.2 Interrupts

In the FPGA the following interrupt sources are managed:
– VME-ACFAIL
– VME-SYSFAIL
– VME-BUSERROR
– VME-IRQ7.. VME_IRQ1

Via registers INTENA/B/C any assignment to the CPU interrupt inputs can be made.

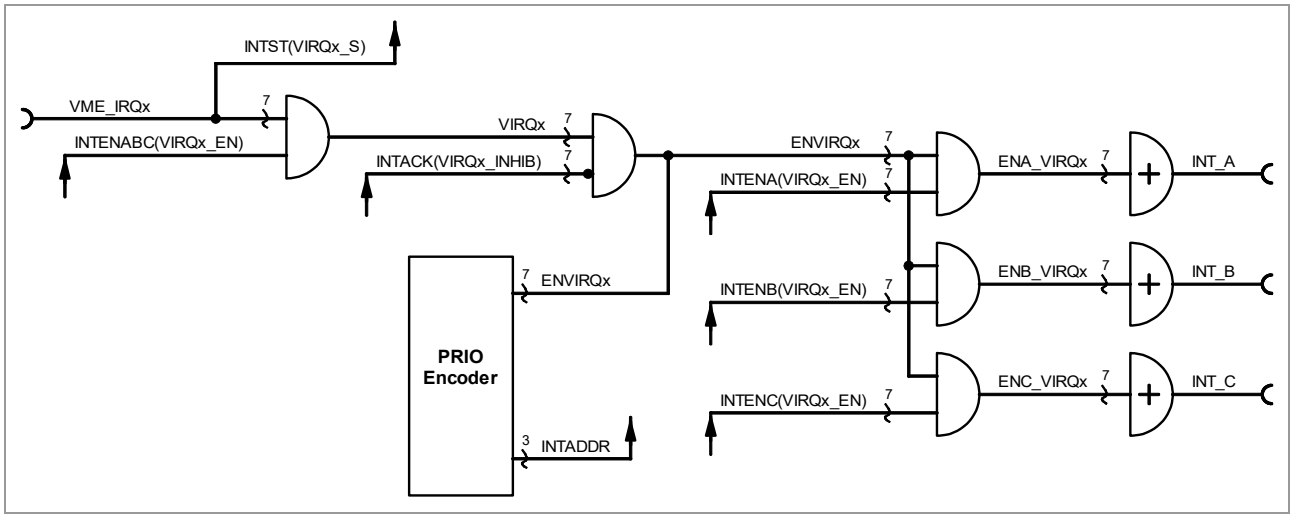


Figure 18: Assignment of the interrupts

9.3.3 Handling of the Vector Interrupts VIRQ7 .. VIRQ1

To proceed the corresponding vector interrupt, a so called IACK access has to be made.
In register INTADDR the vector address of the highest priority interrupt level is written.
A read access to “Interrupt_Ack” (PCIe Base Adress Bar 0 + Offset 0x2 0000) + (INTADDR) generates the corresponding VMEbus access.
When address “Interrupt_Ack” + 0 is accessed, the highest priority interrupt is processed automatically.
If an 8-bit read access is made, only the 8-bit vector is returned.
If a 16-bit access is made, the vector is contained in the lower 8-bit and the interrupt level is coded in the higher byte (bit 8+level = 1).

Example:
0x4090: Vector = 0x90, Level=6

9.3.4 “Inhibit-Mode”

For a better support of “RORA” interrupts (Release On Register Access) the interrupt handler can operate in the “Inhibit-Mode”. (INTINHEN Bitx=1).

After reading the vector the corresponding VME-Irq-Level is set to “Inhibit” here (register INTACK(BIT Level) = 1) and thus the hardware interrupt in the interrupt handler is reset.
The software now proceeds the interrupt on user level.
After the interrupt handling the corresponding level has to be enabled again.
For this, the value of the interrupt level (here: 0x40) is used, which has been read during the interrupt acknowledge cycle and that is written in the register INTACK.
The status “Inhibit” can also be caused for the local interrupts (by writing on INTINHEN).

10. User LED Configuration

Configuration register 8-bit, accessible via local bus with offset 0x100:
The LED-indicator states (green/red/blink) for the CPU_LED and the USER_LED are defined here.

Offset	Access	Short	Register name	Bits							
				Bit 7-0							
				7	6	5	4	3	2	1	0
0x00	R/W	LED_CPU	CPU LED Control	res.		TIME[1…0]		CTRL[3..0]			
0x01	R/W	LED_USER	User LED Control	res.		TIME[1…0]		CTRL[3..0]			
0x02	R	CREL	Core Release Register	REL[3…0]				STEP[3…0]			
0x03	R	ENDN	Endian Register	0x21							

CTRL[3…0]	Function
other	off (default)
0010	green on
0011	green blink
1010	green flashing (fixed time)
0100	red on
0101	red blink
1100	red flashing
0111	alternating blink (fixed time)

TIME[1…0]	blink period
00	200 ms (default)
01	100 ms
10	400 ms
11	800 ms

Table 24: LED_Control

0x00: LED_CPU read/write

0x01: LED_USER read/write

0x02: CREL read_only
Contains the Core Release Info of the block “LED-Control”, subdivided in REL[3:0] and STEP[3:0]

0x03: ENDN read_only
Test register for the check of the Endianness,
fixed 0x21

11. MRAM

The CPU board provides an MRAM with 512 kByte capacity.
It is accessible via register access and memory mapped.

11.1 MRAM Register

Access on the parallel MRAM via register 8-bit, accessible via local bus with offset 0x200:

NOTICE
With this only the lower 64kByte of the MRAM can be accessed!
(Compatibility mode to MVME5110)
Access via the MemoryMapped address range is recommended, see chapter 11.2 “MRAM over MemoryMapped MRAM Access” .

Offset	Access	Short	Register name	Bits							
				Bit 7-0							
				7	6	5	4	3	2	1	0
0x00	R/W	ADDR_LOW	Lower Address (7…0)	ADDR_LOW[7…0]							
0x01	R/W	ADDR_HIGH	Higher Address (15..8)	ADDR_HIGH[7…0]							
0x02	R/W	DATA	Data Register*	DATA[7…0]							
0x03	R	CREL	Core Release Register	REL[3…0]				STEP[3…0]			

*Read data on read access, write data on write access

Table 25: MRAM_Register

0x00: ADDR_LOW read/write

0x01: ADDR_High read/write

0x02: DATA read/write

0x03: CREL read_only
Contains the Core Release Info of the block “MRAM_Register”, divided in REL[3:0] and STEP[3:0]

11.2 MRAM over MemoryMapped MRAM Access

Accessible via local bus with offset: 0x10 0000 (512 kByte, byte-access)

Access to the parallel MRAM in Byte-Mode.
The following transfers are supported: 32Bit/16Bit/8Bit

12. Bootloader

12.1 License

The VME-CPU/T10 module uses the open source bootloader *„Das U-Boot“*. The U-Boot source code is published in terms of the GNU public license (GPL). Please see esd's „3rd party licensor notice“ document that is part of the product's documentation for the full license text. Please contact esd for a copy of the full bootloader source code for the VME-CPU/T10.
The U-Boot source is available from esd on request.

12.2 Configuration and Console Access

Use the serial cable VME-CPU/T10-Cable_Console (see Order Information, page 63) with RJ45 connector (VME-CPU/T10 side) and DSUB9 connector (PC side) to connect the VME-CPU/T10 to a PCs COM port. The U-Boot console is accessible via the front panel's 'DEBUG' device port (RJ45 socket).
Now open a terminal program and point to the COM port of the VME-CPU/T10.
The default communication parameters are 115 200 baud, 8N1 (8 data bits, no parity, 1 stop-bit, no hardware handshake).

After the next power-on you will see the bootloader start-up messages being output on the serial console. When you see the message 'Press SPACE ....', hit the space key to stop booting and to access the interactive bootloader console. At the prompt you can use an extensive command set to do configuration, debugging or testing tasks. Enter help (followed by hitting the RETURN key) to get a full list of all supported commands.

```
U-Boot 2016.03.02-rc3-17455-g27ab0a9-dirty (Nov 14 2016 - 15:13:48 +0100)

CPU:   T1014, Version: 1.0, (0x85440010)
Core:  e5500, Version: 2.1, (0x80241021)
Clock Configuration:
       CPU0:1200 MHz,
       CCB:400  MHz,
       DDR:700  MHz (1400 MT/s data rate) (Asynchronous), IFC:25   MHz
       QE:200  MHz
       FMAN1: 600 MHz
       QMAN:  400 MHz
L1:    D-cache 32 KiB enabled
       I-cache 32 KiB enabled
Reset Configuration Word (RCW):
       00000000: 080e000c 00000000 00000000 00000000
       00000010: 4a800003 00808002 ec027000 21002000
       00000020: 00000000 00000000 60000000 00033400
       00000030: 00000000 48260a08 00000000 00000006
Board: vmet10/T1014, HW: 0
Boot from SPI
SERDES Reference Clocks:
SD1_CLK1=156.25MHZ, SD1_CLK2=100.00MHZ
I2C:   ready
SPI:   ready
DRAM:  Detected UDIMM esd_CPU-T10_512MB
Found timing match: n_ranks 1, data rate 1666, rank_gb 0
        clk_adjust 14, wrlvl_start 8, wrlvl_ctrl_2 0x809090b, 0 of 1 controllers are
interleaving.
512 MiB (DDR3, 64-bit, CL=10, ECC on)
L2:    256 KiB enabled
Corenet Platform Cache: 256 KiB enabled
Using SERDES1 Protocol: 149 (0x95)
MMC:   FSL_SDHC: 0
PCIe1: Root Complex, no link, regs @ 0xfe240000
PCIe1: Bus 00 - 00
```

```
PCIe2: Root Complex, x1 gen1, regs @ 0xfe250000
PCI Scan: Found Bus 2, Device 0, Function 0
  02:00.0     - 12fe:5410 - Bridge device
PCIe2: Bus 01 - 02
PCIe3: Root Complex, no link, regs @ 0xfe260000
PCIe3: Bus 03 - 03
In:    serial
Out:   serial
Err:   serial
Found FPGA at PCI device 02.00.0:
FPGA Version 1.0.0002 build 2016-11-03  15:42:41 UTC
Net:   Fman1: Uploading microcode version 106.4.17
FM1@DTSEC3, FM1@DTSEC4 [PRIME]
PARAM: @1fc00000
memsize=0x20000000, base=0x20000000
do_painit 538 nextbase 0x1fffe000 size 0x1000
Hit any key to stop autoboot:  0
```

13. EU-Declaration of Conformity

EU-KONFORMITÄTSERKLÄRUNG
EU DECLARATION OF CONFORMITY

Adresse / *Address*
esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover
Germany

esd erklärt, dass das Produkt *esd declares, that the product*	Typ, Modell, Artikel-Nr. *Type, Model, Article No.*
VME-CPU/T10	**V.1940.01**
VME-CPU/T10-F	**V.1940.02**
die Anforderungen der Normen *fulfills the requirements of the standards*	**EN 61000-6-2:2005,** **EN 61000-6-4:2007/A1:2011**
gemäß folgendem Prüfbericht erfüllt. *according to test certificate.*	**H-K00-0663-17**
Das Produkt entspricht damit der EU-Richtlinie „EMV" *Therefore the product conforms to the EU Directive 'EMC'*	**2014/30/EU**
Das Produkt entspricht den EU-Richtlinien „RoHS" *The product conforms to the EU Directives 'RoHS'*	**2011/65/EU, 2015/863/EU**

Diese Erklärung verliert ihre Gültigkeit, wenn das Produkt nicht den Herstellerunterlagen entsprechend eingesetzt und betrieben wird, oder das Produkt abweichend modifiziert wird.
This declaration loses its validity if the product is not used or run according to the manufacturer's documentation or if non-compliant modifications are made.

Name / *Name*	T. Bielert
Funktion / *Title*	QM-Beauftragter / *QM Representative*
Datum / *Date*	Hannover, 2018-12-03

Rechtsgültige Unterschrift / *authorized signature*

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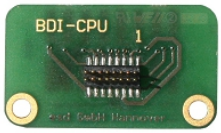
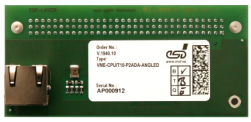
14. Order Information

Type	Properties	Order No.
VME-CPU/T10	VME Master with PPC QorIQ T1022, 1,2 GHz 2x XMC/PMC Slots, 2x GBit-Ethernet	V.1940.01
VME-CPU/T10-F	VME Master with PPC QorIQ T1014, 1,2 GHz	V.1940.02
Accessories		
VME-CPU/T10-Cable_Console	Cable DSUB9 <-> RJ45 for RS232 Debug-Interface length: ca. 0.5 m	V.1940.12
CPU-ADAPTER-BDI 	Interface to connect the Abatron BDI2000 and BDI3000 to VME-CPU/T10	V.2029.02
VME-CPU/T10-P2ADA-ANGLED 	VME-CPU/T10-P2ADA-ANGLED P2 Ethernet Adapter for VME-CPU/T10, 90 deg.	V.1940.10
VME-CPU/T10-P2ADA-STRAIGHT 	VME-CPU/T10-P2ADA-STRAIGHT P2 Ethernet Adapter for VME-CPU/T10, 0 deg.	V.1940.11
Software		
Board Support Packages		
VME-CPU/T10-Linux-BSP	Linux Board Support Package, incl. 12 months support	V.1940.57
VME-CPU/T10-QNX-BSP	QNX Board Support Package, incl. 12 months support	V.1940.55
VME-CPU/T10-OS9-BSP	OS-9 Board Support Package, incl. 12 months support	V.1940.56
VME-CPU/T10-VxW-BSP	VxWorks Board Support Package, incl. 12 months support	V.1940.58
Support for BSP		
VME-CPU/T10-Linux-Support	Hotline Support and Linux BSP Updates, for 12 months	V.1940.67
VME-CPU/T10-QNX-Support	Hotline Support and QNX BSP Updates, for 12 months	V.1940.65
VME-CPU/T10-OS9-Support	Hotline Support and OS-9 BSP Updates, for 12 months	V.1940.66
VME-CPU/T10-VxW-Support	Hotline Support and VxWorks BSP Updates, for 12 months	V.1940.68

Order Information

EtherCAT Master		
EtherCAT Master - Linux/PowerPC	EtherCAT Master Stack for Linux, Object code, Runtime license for a single site	P.4500.03
EtherCAT Master - QNX 6.x/PowerPC	EtherCAT Master Stack for QNX 6.x, Object code, Runtime license for a single site	P.4500.10
EtherCAT Master - OS-9 5.2/PowerPC	EtherCAT Master Stack for OS-9 5.2, Object code, Runtime license for a single site	P.4500.40
EtherCAT Master - VxW/PowerPC	EtherCAT Master Stack for VxWorks Object code, Runtime license for a single site	P.4500.20

For detailed information about the driver availability for your special operating system, please contact our sales team.

Table 26: Order information

PDF Manuals

Please download the manual as PDF document from our esd website www.esd.eu for free.

Manuals		Order No.
VME-CPU/T10-ME	Hardware Manual in English to VME-CPU/T10 and VME-CPU/T10-F	V.1940.21

Table 27: Available manuals

Printed Manuals

If you need a printout of the manual additionally, please contact our sales team: sales@esd.eu for a quotation. Printed manuals may be ordered for a fee.