PCIe-XPIMC-Carrier

XMC/PMC/PIM Carriers for PCIe

Hardware Manual

to Product V.2100.01, V.2100.02

esd electronic system design gmbh
Vahrenwalder Str. 207 • 30165 Hannover • Germany
http://www.esd.eu
Phone: +49 (0) 511 3 72 98-0 • Fax: +49 (0) 511 3 72 98-68

N O T E

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esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover
Germany

Phone:	+49-511-372 98-0
Fax:	+49-511-372 98-68
E-Mail:	info@esd.eu
Internet:	www.esd.eu

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Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Revision	Chapter	Changes versus previous version	Date
1.0	-	First release	2011-11-18
1.1	-	Added new Safety Instructions	2012-08-14
	2.1	Add new graphic	
	8	Added Declaration of Conformity	
1.2	2.1	Updated PCB top view graphic	2012-11-26
	8	Updated chapter 'Declaration of Conformity'	
	10	Updated chapter 'Order Information'	

Technical details are subject to change without further notice.

Safety Instructions

- When working with PCIe-XPIMC-Carrier follow the instructions below and read the manual carefully to protect yourself from injury and the PCIe-XPIMC-Carrier from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- The device has to be securely installed in the control cabinet before commissioning.
- Protect the PCIe-XPIMC-Carrier from dust, moisture and steam.
- Protect the PCIe-XPIMC-Carrier from shocks and vibrations.
- The PCIe-XPIMC-Carrier may become warm during normal use. Always allow adequate ventilation around the PCIe-XPIMC-Carrier and use care when handling.
- Do not operate the PCIe-XPIMC-Carrier adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and objects.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The PCIe-XPIMC-Carrier may only be driven by power supply current circuits, that are contact protected.
  A power supply, that provides a safety extra-low voltage (SELV or PELV) according to EN 60950-1, complies with this conditions.

Attention !
Electrostatic discharges may cause damage to electronic components.
To avoid this, please perform the steps described on page 11 *before* you touch the PCIe-XPIMC-Carrier, in order to discharge the static electricity from your body.

Qualified Personal
This documentation is directed exclusively towards personal qualified in control and automation engineering. The installation and commissioning of the product may only be carried out by qualified personal, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity
The PCIe-XPIMC-Carrier is an industrial product and meets the demands of the EU regulations and EMC standards printed in the conformity declaration at the end of this manual.

Warning: In a residential, commercial or light industrial environment the PCIe-XPIMC-Carrier may cause radio interferences in which case the user may be required to take adequate measures.

Intended Use
The intended use of the PCIe-XPIMC-Carrier is the operation as PMC or XMC carrier in a PCI Express system.
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The PCIe-XPIMC-Carrier is intended for installation in a PCIe system only.
- The operation of the PCIe-XPIMC-Carrier in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the PCIe-XPIMC-Carrier for medical purposes is prohibited.

Service Note
The PCIe-XPIMC-Carrier does not contain any parts that require maintenance by the user.

Disposal
Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

Table of contents

1. Overview

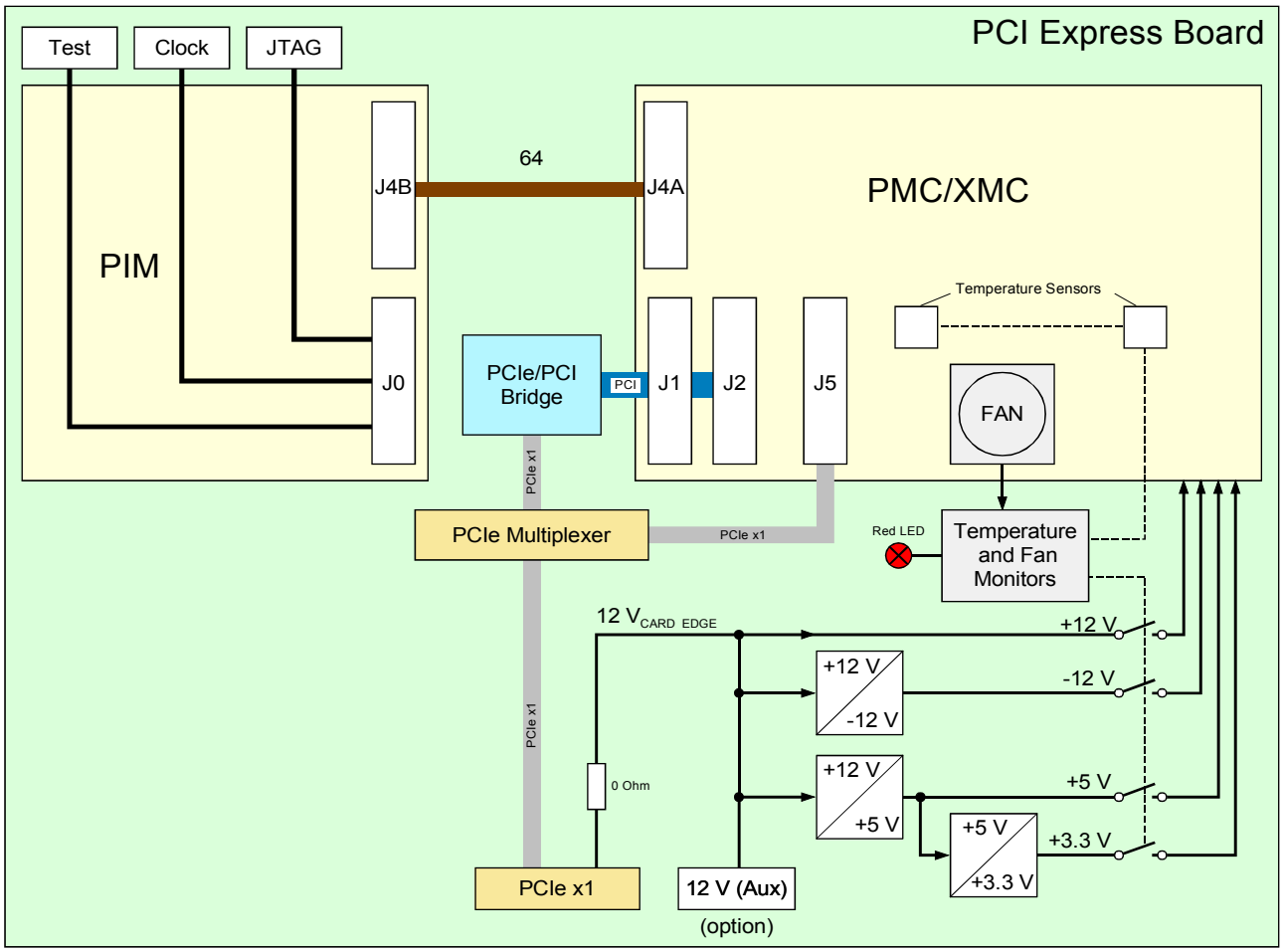


Figure 1: Block circuit diagram

The PCIe-XPIMC-Carrier is a PCIe 1x board that can carry a single PMC or alternatively a XMC module. The PMCs PCI interface is connected to the boards PCIe card edge interface through a single lane (1x) PCI/PCIe bridge. When using a XMC module its first PCIe lane is connected to the card edge connector.
I/O connectivity is achieved by adding a PIM module slot (acc. Vita 36). All 64 I/O signals from the PMC/XMC J4 are routed directly to the PIM's J4 connector.
Some PIM J0 signals have a special functionality as already implemented in the PMC-Box [1].
The board is designed for a PCIe 1x slot. All installed modules are power supplied through the 12V power rail. For extreme high power applications an external power source (12V) can optionally be installed. The 12V auxiliary connector Aux Power is doubled (IN+OUT) to allow daisy chaining multiple carriers on huge PCIe backplanes.

The carrier board is available in two versions:

- *Normal (forward) version*: the PIM slot is placed at the slot bracket side and the PMC/XMC is oriented towards the system's centre.
- *Reverse version:* the PMC/XMC slot is placed at the slot bracket side and the PIM is oriented towards the system's centre.

2. PCB View with Connectors

2.1 Normal Version

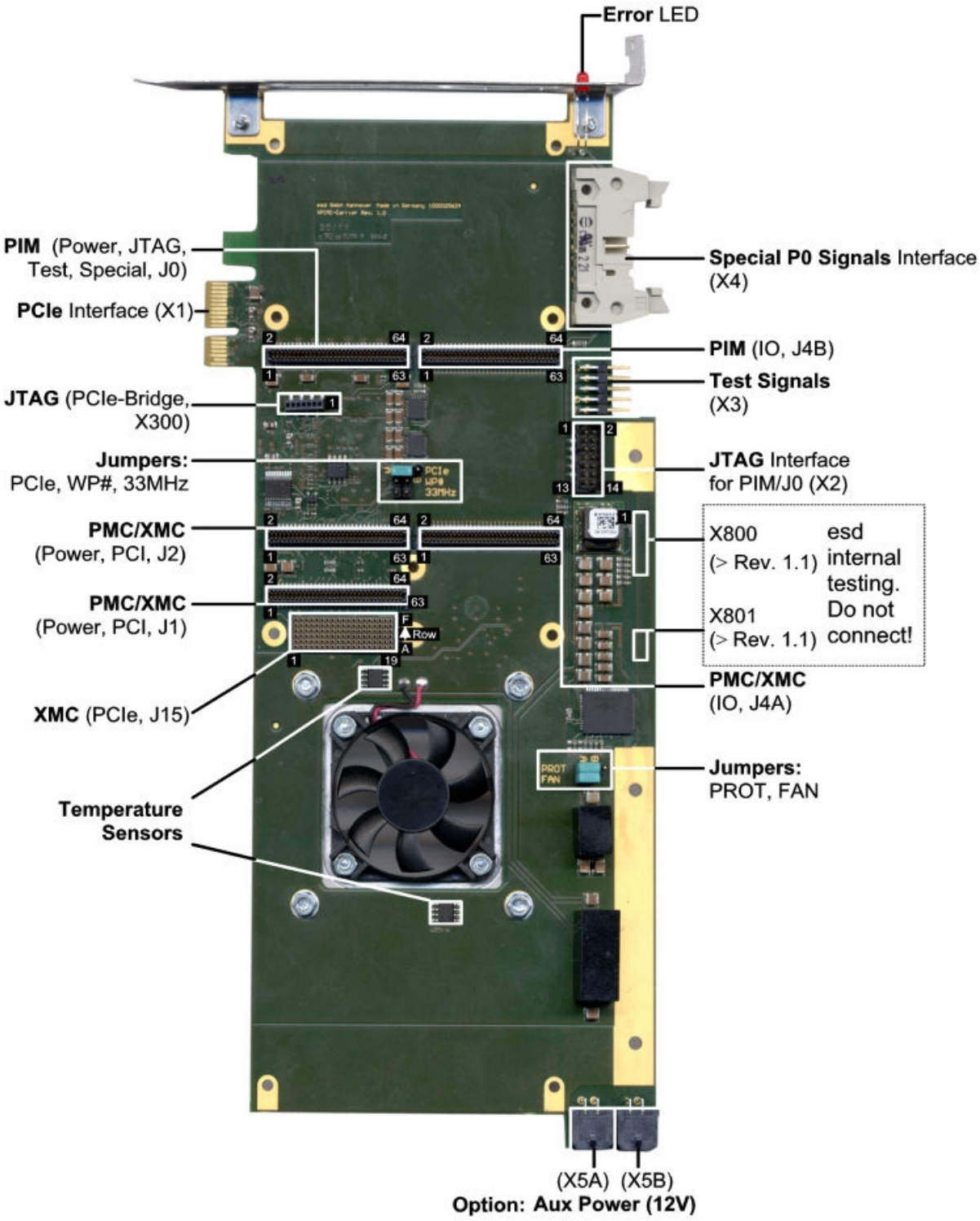


Figure 2: PCB top view (normal version)

- No parts are placed under the PIM module.
- Mounting holes are placed at the upper edge of the board.

See also page 16 for signal assignment of the connectors.

2.2 Component Placement of Reverse Version

- The positions of the connectors JTAG, Test, Aux Power and Clock in the PCIe-XPIMC(reverse)-Carrier are the same as in the normal version (see Figure: 2). The signal assignment of these connectors is described from page 16.

- The jumpers PROT and FAN are positioned between the connectors X4 and X3.

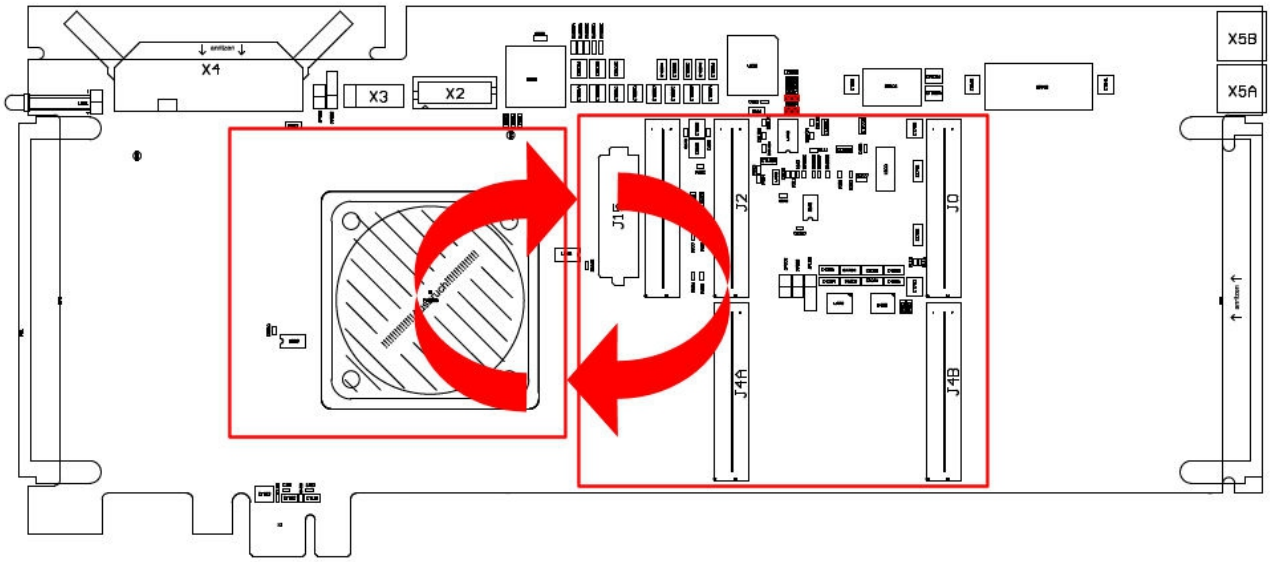


Figure 3: Component placement specification of PCIe-XPIMC(reverse)-Carrier

- The reverse version has the PMC/XMC and PIM sites swapped, so that the PMC/XMC bezel is accessible via the slot bracket (see Figure: 3).

- The position of the connectors J0, J1, J2, J4A, J4B, J15 and X300 and the pin position of these connectors is described in Figure: 4 (page 9).

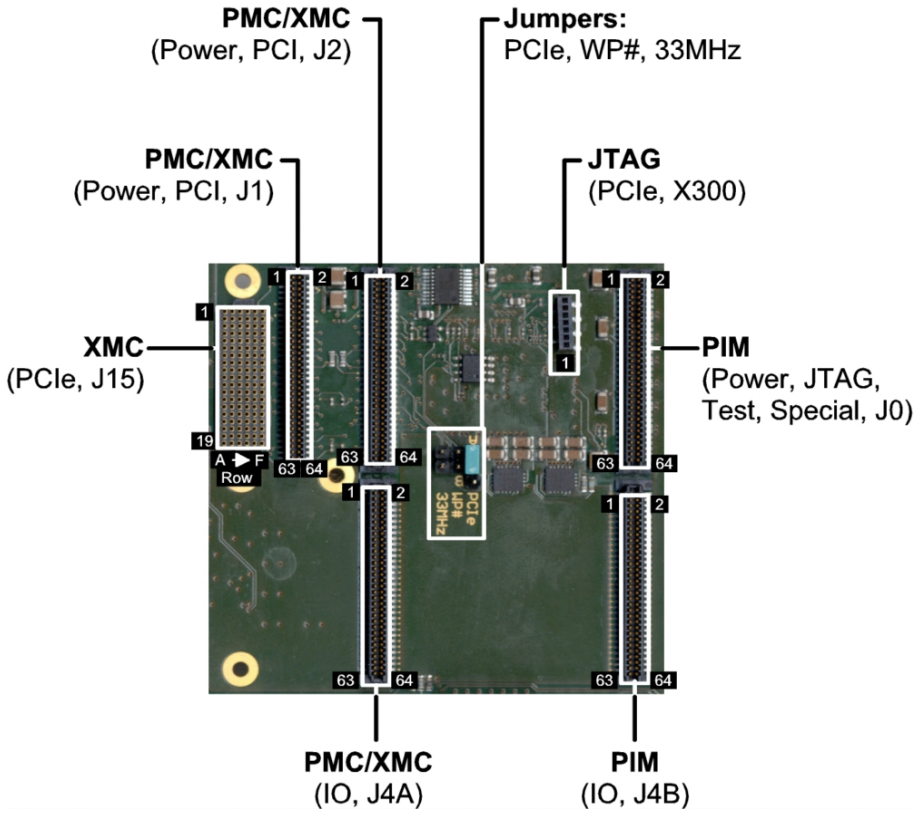


Figure 4: Position of connectors and pins of PCIe-XPIMC(reverse)-Carrier (detail)

3. Hardware Configuration

The XPIMC-Carrier is equipped with 5 jumpers.

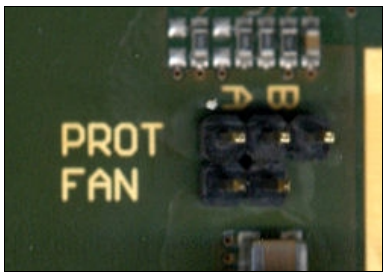


Figure 5: Jumpers PROT and FAN (detail, normal version)

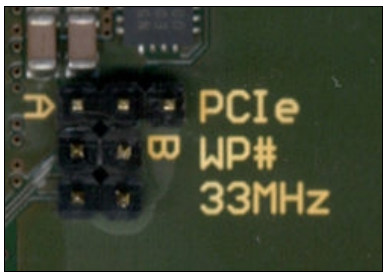


Figure 6: Jumpers PCIe, WP# and 33MHz (detail)

Jumpers with two male contacts: FAN, WP# and 33MHz
These jumpers can be installed or not installed.

Name	Jumper Installed	Jumper Not Installed	Default	Jumper Name in PCB
FAN	fan enabled	fan disabled	installed	JP900
WP#	PCIe/PCI bridge configuration EEPROM, write enabled	PCIe/PCI bridge configuration EEPROM, write protected	not installed	JP310
33MHz	PCI Bus forced to 33 MHz operation	speed is selected by PMC's M66EN signal	not installed	JP500

Jumpers with three male contacts: PCIe and PROT
These jumpers can be not installed or installed to POS A or POS B.

Name	Jumper POS A	Jumper POS B	Jumper Not Installed	Default	Jumper Name in PCB
PROT	full protection enabled (fan and temperature)[1]	only temperature observation	protection disabled	POS A	JP920
PCIe	Auto select by XMC-PRESET pin	PCIe connected to XMC site	PCIe connected to PCIe/PCI bridge	POS A	JP100

1 This option is only available on the Carriers's hardware revision 1.0. Beginning with the revision 1.1, the jumper only has two contacts.

4. Hardware Installation

Read the safety instructions at the beginning of this document carefully, before you start with the hardware installation!

Danger!
Electric shock risk. Never carry out work while power supply voltage is switched on!

Attention !
Electrostatic discharges may cause damage to electronic components. To avoid this, please discharge the static electricity from your body by touching the metal case of the PCI Express system *before* you touch the PCIe-XPIMC-Carrier.

Procedure:

1. Switch off your computer and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. If not already done, plug on the PMC/XMC module and PIM module, which are to be used.
4. Disconnect the computer from the mains.
   If the computer does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (i.e. with caution label).

   Danger!
   Never carry out work while power supply voltage is switched on!
5. Open the case.
6. Insert the PCIe-XPIMC-Carrier board into the selected PCIe slot. Carefully push the board down until it snaps into place. It is strongly recommended to install additional mounting brackets due to the high mass of of a PCIe-XPIMC-Carrier with installed PIM and PMC/XMC modules. Care must be taken especially during transport of the PC with installed PCI-XPIMC-Carriers.
7. Close the computer case again.
8. Connect the interfaces in the front panel of the PCIe-XPIMC-Carrier via the connectors. The type of interface and connector depends on the PIM or PMC/XMC board used.
9. Connect the computer to mains again (mains connector or safety fuse).
10. Switch on the computer and the peripheral devices.
11. End of hardware installation.

5. LEDs

5.1 Position of the LED

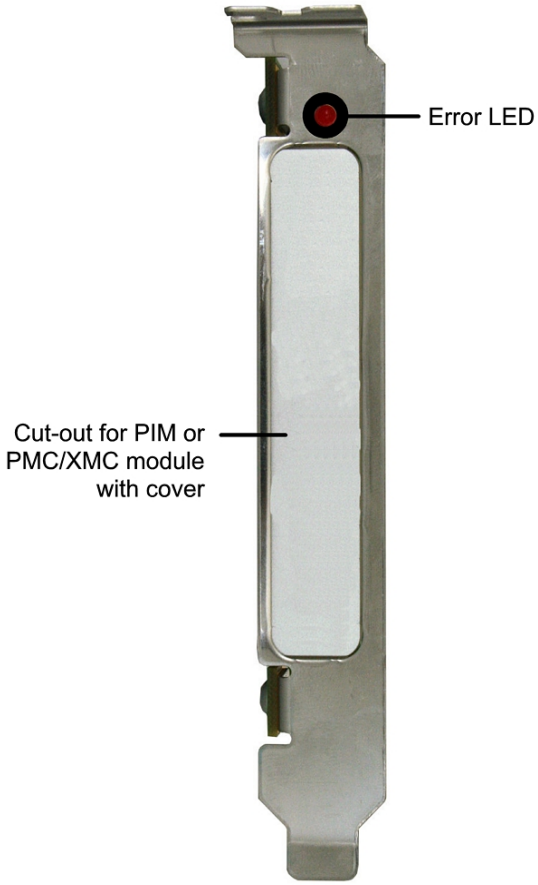


Figure 7: Connectors and LEDs

5.2 LED Indication

LED	Colour	Function	Indicator State	Description	LED name in schematic diagram
Error	red	Fan or Temperature Error	off	normal operation	LED1
			on	fan or temperature error condition. The LED behavior is uneffected by PROT jumper status.	

Table 1: Description of LED

6. Technical Data

6.1 General Technical Data

Power supply	nominal voltage: 3.3 V / 12 V via PCIe card edge connector nominal current without PMC/XMC or PIM module: 3.3 V: < 10 mA 12 V: approx. 220 mA		
Connectors	X1	PCIe 1x card edge	PCB card edge
	J1	PMC / XMC (Power, PCI)	PMC connector, 64-pin
	J2	PMC / XMC (Power, PCI)	PMC connector, 64-pin
	J4A	PMC / XMC (I/O)	PMC connector, 64-pin
	J15	XMC (PCIe)	XMC connector, 6x19-pin
	J4B	PIM (I/O)	PMC connector, 64-pin
	J0	PIM (Power, JTAG, Test, Special)	PMC connector, 64-pin
	X2	JTAG interface	(Molex, 87832-1420, (2x7 pin, 2mm)
	X3	Test signals	(2 x 5., 2.54 mm 2-row strip connector, angled)
	X4	Clock	(ODU Flakafix, Series 511, or similar (DIN41651), angled, 14 pole, engagement hooks)
	X5a/b	Aux Power (12V) in + out	2 x Molex, MicroFit, 2 x 2 pole, part# 0430450400 / 0430450401
Temperature range	0°C .. +50°C ambient temperature		
Humidity	max. 90%, non-condensing		
Dimensions	~98 mm x ~250 mm		
Weight	155 g		

Table 2: General data of the module

6.2 PCI/PCIe Interface

PCI signal multiplexer type	PI2PCIE2212, Pericom
PCI-PCIe-bridge type	PI7C9X111SL, Pericom
PCI specification	33/66MHz, 32bit
Lane	1x
PCIe SMBus	The SMBus on the card edge connector is not used by the design.

Table 3: Data of PCI/PCIe interface

6.3 PMC/XMC Interface

Number	1x PMC or XMC depending on position of the PCIe jumper
Standard	PMC: IEEE Std. 1386-2001, IEEE 1386.1-2001 XMC: VITA 42.10
PMC/XMC card size	one single-size module
Signal voltage level	PMC: Universal, 3.3V PCI signalling, with 5 V tolerance
Bus system	XMC: PCI Express
Connectors	J1 PMC / XMC (Power, PCI) J2 PMC / XMC (Power, PCI) J4a PMC / XMC (I/O) J15 XMC (PCIe)

Table 4: Data of PMC interface

6.4 PIM

Number	1
Standard	acc. to Vita 36d0.1
PIM card size	one single-size module
Connectors	J0, J4b

Table 5: Data of PIM interface

6.5 Power Supply, Fan and Monitoring

Supply voltage	3.3V / 12V via PCIe card edge connector
Power consumption	A total power consumption of 25W must not be exceeded. Maximum allowed power consumption also heavily depends on adequate cooling/airflow. Max. current on logic power rails: I_{max}(3.3V) = 5A I_{max}(5V) = 5A Max. current on auxiliary power rails: I_{max}(+12V) = 400mA I_{max}(-12V) = -150mA Per default main power will be taken from PCIe card edge's 12V rail. As an option 12V supply rail can be alternatively fed from an external source through an auxiliary connector (see chapter 7.9). In this situation the 12V connection to the card edge has to be disconnected by removing 0-Ohm resistors. See block diagram for details on internal power supply rails (Figure 1)
Over current protection	none, all supply rails are short circuit protected
Thermal protection	2x DS1631A under PMC/XMC site The upper threshold is programmed to 60°C.
Fan placement	fan is placed below PMC/XMC site.
Fan type	Sunon, 40mm x 40mm x 6mm (GM0504PEV1-8.GN)
Fan control	none, full speed
Fan monitoring	current sense
Protection circuit	PIM, PMC/XMC and PCIe/PCI bridge are turned off in case of an over temperature condition. A power cycle of the carrier is required to return to normal operation. In case of a fan or temperature error the red LED is turn on.

7. Connector Assignments

7.1 J0 – PIM Connector

Signal	Pin	Pin	Signal
n.c.	1	2	+12V
PIM.TMS	3	4	n.c.
+5V	5	6	n.c.
PIM.TCK	7	8	n.c.
n.c	9	10	+3.3V
n.c.	11	12	DPSG.1.N
GND	13	14	DPSG.1.P
PIM.TDO	15	16	n.c
PIM.TDI	17	18	GND
PIM.TRST#	19	20	DPSG.2.N
+5V	21	22	DPSG.2.P
n.c	23	24	n.c.
n.c.	25	26	+3.3V
n.c.	27	28	DPSG.3.N
GND	29	30	DPSG.3.P
n.c	31	32	n.c
n.c.	33	34	GND
PM-T1	35	36	DPSG.4.N
+5V	37	38	DPSG.4.P
PM-T2	39	40	n.c.
PM-T3	41	42	+3.3V
PM-T4	43	44	DPSG.5.N
GND	45	46	DPSG.5.P
n.c.	47	48	n.c.
n.c.	49	50	GND
PM-T5	51	52	TIME_N
+5V	53	54	TIME_P
PM-T6	55	56	n.c.
PM-T7	57	58	+3.3V
PM-T8	59	60	n.c.
-12V	61	62	SCL
n.c.	63	64	SDA

Note:
SCL/SDA are connected to any I²C capable component on the carrier. This includes the thermal sensors (2 x DS1631A).

7.2 J1 – PMC/XMC Connector

Signal	Pin	Pin	Signal
JTAG.TCK	1	2	-12 V
GND	3	4	PCI.INTA#
PCI.INTB#	5	6	PCI.INTC#
PRSNT0#	7	8	+5V
PCI.INTD#	9	10	n.c.
GND	11	12	+3.3V AUX
PCI.CLK	13	14	GND
GND	15	16	PCI.GNT0#
PCI.REQ0#	17	18	+5V
+3.3V	19	20	P-AD31
P-AD28	21	22	P-AD27
P-AD25	23	24	GND
GND	25	26	PCI.C/BE(3)#
P-AD22	27	28	P-AD21
P-AD19	29	30	+5V
+3.3V	31	32	P-AD17
PCI.FRAME#	33	34	GND
GND	35	36	PCI.IRDY#
PCI.DEVSEL#	37	38	+5V
GND	39	40	PCI.LOCK#
+3.3 V via 3.3 kΩ	41	42	+3.3 V via 3.3 kΩ
PCI.PAR	43	44	GND
+3.3V	45	46	P-AD15
P-AD12	47	48	P-AD11
P-AD9	49	50	+5V
GND	51	52	PCI.C/BE(0)#
P-AD6	53	54	P-AD5
P-AD4	55	56	GND
+3.3V	57	58	P-AD3
P-AD2	59	60	P-AD1
P-AD0	61	62	+5V
GND	63	64	+3.3 V via 3.3 kΩ

7.3 J2 – PMC/XMC Connector

Signal	Pin	Pin	Signal
+12 V	1	2	JTAG.TRST#
JTAG.TMS	3	4	JTAG.TD2
JTAG.TD1	5	6	GND
GND	7	8	n.c.
n.c.	9	10	n.c.
+3.3 V via 3.3 kΩ	11	12	+3.3V
PCI.RST#	13	14	GND via 3.3 kΩ
+3.3V	15	16	GND via 3.3 kΩ
PCI.PME#	17	18	GND
P-AD30	19	20	P-AD29
GND	21	22	P-AD26
P-AD24	23	24	+3.3V
P-IDSEL0	25	26	P-AD23
+3.3V	27	28	P-AD20
P-AD18	29	30	GND
P-AD16	31	32	PCI.C/BE2#
GND	33	34	P-IDSEL1
PCI.TRDY#	35	36	+3.3V
GND	37	38	PCI.STOP#
PCI.PERR#	39	40	GND
+3.3V	41	42	PCI.SERR#
PCI.C/BE1#	43	44	GND
P-AD14	45	46	P-AD13
PCI.M66EN	47	48	P-AD10
P-AD8	49	50	+3.3V
P-AD7	51	52	PCI.REQ1#
+3.3V	53	54	PCI.GNT1#
n.c.	55	56	GND
n.c.	57	58	n.c.
GND	59	60	n.c.
+3.3 V via 3.3 kΩ	61	62	+3.3V
GND	63	64	n.c.

7.4 J4A PMC / XMC (I/O) and J4B PIM (I/O) Connectors

The signal assignments of the I/O-connectors J4A and J4B are identical.
The signal pins of the connectors J4A and J4B are 1:1 connected internally. So signals are only passed through.

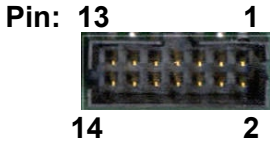
7.5 J15 XMC (PCIe) Connector

Pin	Signal					
	Row A	Row B	Row C	Row D	Row E	Row F
1	PEX. ODATA0.P	PEX. ODATA0.N	+3.3V	n.c.	n.c.	+5V
2	GND	GND	JTAG.TRST#	GND	GND	n.c.
3	n.c.	n.c.	+3.3V	n.c.	n.c.	+5V
4	GND	GND	JTAG.TCK	GND	GND	XMC_RSTO#
5	n.c.	n.c.	+3.3V	n.c.	n.c.	+5V
6	GND	GND	JTAG.TMS	GND	GND	+12V
7	n.c.	n.c.	+3.3V	n.c.	n.c.	+5V
8	GND	GND	JTAG.TD2	GND	GND	-12V
9	n.c.	n.c.	n.c.	n.c.	n.c.	+5V
10	GND	GND	JTAG.TDO	GND	GND	GND
11	PEX.IDATA0.P	PEX.IDATA0.N	n.c.	n.c.	n.c.	+5V
12	GND	GND	GND	GND	GND	LC.XMC_ PRSNT#
13	n.c.	n.c.	3.3V AUX	n.c.	n.c.	+5V
14	GND	GND	+3.3V	GND	GND	SDA
15	n.c.	n.c.	n.c.	n.c.	n.c.	+5V
16	GND	GND	GND	GND	GND	SCL
17	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.
18	GND	GND	n.c.	GND	GND	n.c.
19	PEX.RCLK0.P	PEX.RCLK0.N	n.c.	n.c.	n.c.	n.c.

7.6 X2 – PIM JTAG Connector

Device connector: Molex, 87832-1420, (2x7 pin, 2mm, male contacts)

Pin Position (connector view):



Pin Assignment:

Signal	Pin	Pin	Signal
GND	1	2	+3.3V
GND	3	4	PIM-TMS
GND	5	6	PIM-TCK
GND	7	8	PIM-TDO
GND	9	10	PIM-TDI
GND	11	12	n.c.
GND	13	14	PIM-TRST#

Note:
All JTAG signals are directly routed to the PIM J0 connector.

7.7 X3 – PIM Test Signals

Device Connector: 2 x 5., 2.54 mm 2-row strip connector, male, angled

Pin Position (connector view):

Pin: **9** **1**

10 **2** PCB side

Pin Assignment:

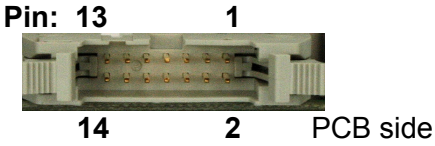
Signal	Pin	Pin	Signal
GND	1	2	PM-T1
PM-T2	3	4	PM-T3
PM-T4	5	6	PM-T5
PM-T6	7	8	PM-T7
PM-T8	9	10	+3.3V

Note:
All test signals are directly routed to the PIM J0 connector.

7.8 X4 – Special P0 Signals

Device Connector: ODU Flakafix, Series 511, or similar (DIN41651), angled, 14 pole, male engagement hooks

Pin Position (connector view):



Pin Assignment:

Signal	Pin	Pin	Signal
DPSG.1.N	1	2	DPSG.1.P
DPSG.2.N	3	4	DPSG.2.P
DPSG.3.N	5	6	DPSG.3.P
GND	7	8	GND
DPSG.4.N	9	10	DPSG.4.P
DPSG.5.N	11	12	DPSG.5.P
TIME_N (IRIG-B digital)	13	14	TIME_P (IRIG-B digital)

Note 1:
All signals are routed for differential signalling.

Note 2:
All signal pairs are terminated by a series network (100R + 1nF)

Note 3:
All test signals are directly routed to the PIM J0 connector

7.9 Option: X5A/B – Aux Power (12V)

Device Connectors: 2 x Molex, MicroFit, 2 x 2 pole, male,
part# 0430450400 / 0430450401

Pin Position (Connector view):

Connector: X5A X5B
Pin: **4 3** **4 3**

2 1 **2 1** PCB side

The Aux Power connectors X5A and X5B are assigned with the same signals.

Pin Assignment:

Signal	Pin	Pin	Signal
GND	4	3	GND
+12V_aux	2	1	+12V_aux

X5A/B are are optional and not installed per default. Per default the 12 V power supply voltage is supplied via the card edge connector. When X5A/B are used to supply the board the +12V rail on the card edge must be disconnected. Please contact esd for instructions.

8. Declaration of Conformity

EG-KONFORMITÄTSERKLÄRUNG
EC DECLARATION OF CONFORMITY

Adresse / *Address*
esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover
Germany

esd erklärt, dass das Produkt *esd declares, that the product*	Typ, Modell, Artikel-Nr. *Type, Model, Article No.*
PCIe-XPIMC-Carrier	**V.2100.01**
PCIe-XPIMC(reverse)-Carrier	**V.2100.02**

die Anforderungen der Normen *fulfills the requirements of the standards*	**EN 61000-6-2:2005,** **EN 61000-6-4:2007+A1:2011**
gemäß folgendem Prüfbericht erfüllt. *according to test certificate.*	**H-K00-0469-12**
Das Produkt entspricht damit der EG-Richtlinie „EMV" *Therefore the product corresponds to the EC-Directive 'EMC'*	**2004/108/EG**
Das Produkt entspricht der EG-Richtlinie „RoHS" *The product corresponds to the EC-Directive 'RoHS'*	**2011/65/EU**

Diese Erklärung verliert ihre Gültigkeit, wenn das Produkt nicht den Herstellerunterlagen entsprechend eingesetzt und betrieben wird, oder das Produkt abweichend modifiziert wird.
This declaration loses its validity if the product is not used or run according to the manufacturer's documentation or if non-compliant modifications are made.

Name / *Name*	T. Ramm
Funktion / *Title*	CE-Koordinator / *CE Coordinator*
Datum / *Date*	Hannover, 2012-11-08

Rechtsgültige Unterschrift / *authorized signature*

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9. References

[1] PCIe base specification, Rev. 1.1
[2] PCI local bus specification, Rev. 3.0
[3] PMC – IEEE 1386
[4] XMC specification (Vita 42.0)
[5] PIM specification (Vita 36 – 199X)
[6] PCIe electromechanical specification, Rev. 2.0

10. Order Information

Type	Properties	Order No.
PCIe-XPIMC-Carrier	XMC/PMC/PIM Carrier with PIM oriented to slot bracket	V.2100.01
PCIe-XPIMC(reverse)-Carrier	XMC/PMC/PIM Carrier with XMC/PMC oriented to slot bracket	V.2100.02

Table 6: Order information

PDF Manuals
Manuals are available in English and usually in German as well. For availability of English manuals see table below.
Please download the manuals as PDF documents from our esd website www.esd.eu for free.

Manuals		Order No.
PCIe-XPIMC-Carrier-ME	Hardware manual in English	V.2100.21

Table 7: Available manuals

Printed Manuals
If you need a printout of the manual additionally, please contact our sales team: sales@esd.eu for a quotation. Printed manuals may be ordered for a fee.